Zhi-Wen Lin

List of Publications by Year
in descending order

161 papers	2,257 citations	331670 21 h-index	315739 38 g-index
162 all docs	162 docs citations	162 times ranked	588 citing authors

#	Article	IF	Citations
1	Mixed-Cell-Height Placement With Drain-to-Drain Abutment and Region Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1103-1115.	2.7	3
2	Topological Structure and Physical Layout Co-Design for Wavelength-Routed Optical Networks-on-Chip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2237-2249.	2.7	2
3	Timing-Aware Fill Insertions With Design-Rule and Density Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3529-3542.	2.7	2
4	Mixed-Cell-Height Placement With Complex Minimum-Implant-Area Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 4639-4652.	2.7	1
5	Voronoi Diagram Based Heterogeneous Circuit Layout Centerline Extraction for Mask Verification. , 2022, , .		0
6	High-Correlation 3D Routability Estimation for Congestion-guided Global Routing. , 2022, , .		4
7	A Bridge-based Compression Algorithm for Topological Quantum Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, , 1-1.	2.7	0
8	Novel Proximal Group ADMM for Placement Considering Fogging and Proximity Effects. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, , 1-1.	2.7	0
9	Mixed-Cell-Height Detailed Placement Considering Complex Minimum-Implant-Area Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2128-2141.	2.7	9
10	Analytical Placement Considering the Electron-Beam Fogging Effect. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 560-573.	2.7	4
11	A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 533-546.	2.7	11
12	Timing-Driven Placement for FPGAs with Heterogeneous Architectures and Clock Constraints. , 2021, , .		3
13	A Bridge-based Compression Algorithm for Topological Quantum Circuits. , 2021, , .		3
14	VLSI Structure-aware Placement for Convolutional Neural Network Accelerator Units. , 2021, , .		4
15	Simultaneous Pre- and Free-assignment Routing for Multiple Redistribution Layers with Irregular Vias. , 2021, , .		3
16	Two-Stage Neural Network Classifier for the Data Imbalance Problem with Application to Hotspot Detection. , 2021, , .		1
17	A Row-Based Algorithm for Non-Integer Multiple-Cell-Height Placement. , 2021, , .		1
18	Via-based Redistribution Layer Routing for InFO Packages with Irregular Pad Structures. , 2020, , .		8

#	Article	IF	Citations
19	A Provably Good Wavelength-Division-Multiplexing-Aware Clustering Algorithm for On-Chip Optical Routing. , 2020, , .		8
20	Time-Division Multiplexing Based System-Level FPGA Routing for Logic Verification. , 2020, , .		4
21	Latch Clustering for Timing-Power Co-Optimization. , 2020, , .		2
22	Topological Structure and Physical Layout Codesign for Wavelength-Routed Optical Networks-on-Chip. , 2020, , .		5
23	An Efficient EPIST Algorithm for Global Placement with Non-Integer Multiple-Height Cells. , 2020, , .		3
24	Unified Redistribution Layer Routing for 2.5D IC Packages. , 2020, , .		2
25	Mixed-Cell-Height Legalization Considering Technology and Region Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5128-5141.	2.7	9
26	Clock-Aware Placement for Large-Scale Heterogeneous FPGAs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5042-5055.	2.7	17
27	Hamiltonian Path Based Mixed-Cell-Height Legalization for Neighbor Diffusion Effect Mitigation. , 2020, , .		3
28	DSA-Compliant Routing for 2-D Patterns Using Block Copolymer Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 267-280.	2.7	0
29	BiG. , 2019, , .		6
30	Analytical Mixed-Cell-Height Legalization Considering Average and Maximum Movement Minimization. , 2019, , .		11
31	Provably Good Maxâ€“Min- m -Neighbor-TSP-Based Subfield Scheduling for Electron-Beam Photomask Fabrication. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 378-391.	3.1	2
32	NTUplace4dr: A Detailed-Routing-Driven Placer for Mixed-Size Circuit Designs With Technology and Region Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 669-681.	2.7	37
33	Mixed-cell-height placement considering drain-to-drain abutment. , 2018, , .		10
34	Mixed-cell-height legalization considering technology and region constraints. , 2018, , .		12
35	Mixed-cell-height placement with complex minimum-implant-area constraints. , 2018, , .		16
36	Efficient Multi-Layer Obstacle-Avoiding Region-to-Region Rectilinear Steiner Tree Construction. , 2018, , .		4

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37	DSA-Friendly Detailed Routing Considering Double Patterning and DSA Template Assignments. , 2018, , .		0
38	Generalized Augmented Lagrangian and Its Applications to VLSI Global Placement. , 2018, , .		3
39	An effective legalization algorithm for mixed-cell-height standard cells. , 2017, , .		34
40	Fogging Effect Aware Placement in Electron Beam Lithography. , 2017, , .		7
41	Toward Optimal Legalization for Mixed-Cell-Height Circuit Designs. , 2017, , .		38
42	An Interview With Professor Chenming Hu, Father of 3D Transistors. IEEE Design and Test, 2017, 34, 90-96.	1.2	0
43	A novel damped-wave framework for macro placement. , 2017, , .		12
44	Clock-aware placement for large-scale heterogeneous FPGAs. , 2017, , .		9
45	Blockage-aware terminal propagation for placement wirelength minimization. , 2017, , .		0
46	Mixed-cell-height detailed placement considering complex minimum-implant-area constraints. , 2017, , .		11
47	Cut Redistribution With Directed-Self-Assembly Templates for Advanced 1-D Gridded Layouts. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 2066-2079.	2.7	0
48	An integrated-spreading-based macro-refining algorithm for large-scale mixed-size circuit designs. , 2017, , .		3
49	Graph-Based Logic Bit Slicing for Datapath-Aware Placement. , 2017, , .		5
50	Minimum-implant-area-aware detailed placement with spacing constraints. , 2016, , .		19
51	Recent research development and new challenges in analog layout synthesis. , 2016, , .		31
52	Circular-contour-based obstacle-aware macro placement. , 2016, , .		12
53	Cut redistribution with directed self-assembly templates for advanced 1-D gridded layouts. , 2016, , .		10
54	Detailed-routability-driven analytical placement for mixed-size designs with technology and region constraints. , 2015, , .		13

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55	Stitch-Aware Routing for Multiple E-Beam Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 471-482.	2.7	5
56	Non-stitch triple patterning-aware routing based on conflict graph pre-coloring. , 2015, , .		5
57	Detailed-Routing-Driven analytical standard-cell placement. , 2015, , .		15
58	Simultaneous EUV flare variation minimization and CMP control with coupling-aware dummification. , 2014, , .		0
59	Fast lithographic mask optimization considering process variation. , 2014, , .		7
60	Efficient and effective packing and analytical placement for large-scale heterogeneous FPGAs. , 2014, , .		17
61	A Novel Layout Decomposition Algorithm for Triple Patterning Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 397-408.	2.7	50
62	Layer minimization in escape routing for staggered-pin-array PCBs. , 2013, , .		2
63	Symmetrical buffered clock-tree synthesis with supply-voltage alignment. , 2013, , .		1
64	TRECO: Dynamic Technology Remapping for Timing Engineering Change Orders. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1723-1733.	2.7	11
65	Statistical thermal modeling and optimization considering leakage power variations. , 2012, , .		2
66	Unified Analytical Global Placement for Large-Scale Mixed-Size Circuit Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1366-1378.	2.7	21
67	An Efficient Pre-Assignment Routing Algorithm for Flip-Chip Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 878-889.	2.7	10
68	Fast Timing-Model Independent Buffered Clock-Tree Synthesis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1393-1404.	2.7	12
69	Native-Conflict and Stitch-Aware Wire Perturbation for Double Patterning Technology. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 703-716.	2.7	19
70	Escape routing for staggered-pin-array PCBs. , 2011, , .		7
71	A SAT-based routing algorithm for cross-referencing biochips. , 2011, , .		6
72	Heterogeneous B[∗]-trees for analog placement with symmetry and regularity considerations. , 2011, , .		3

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73	PRICE: Power reduction by placement and clock-network co-synthesis for pulsed-latch designs. , 2011, , .		4
74	Thermal-Driven Analog Placement Considering Device Matching. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 325-336.	2.7	26
75	Cross-Contamination Aware Design Methodology for Pin-Constrained Digital Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 817-828.	2.7	51
76	Voltage-Drop Aware Analytical Placement by Global Power Spreading for Mixed-Size Circuit Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1649-1662.	2.7	4
77	Native-conflict-aware wire perturbation for double patterning technology. , 2010, , .		17
78	Template-mask design methodology for double patterning technology. , 2010, , .		2
79	Unified analytical global placement for large-scale mixed-size circuit designs. , 2010, , .		4
80	High variation-tolerant obstacle-avoiding clock mesh synthesis with symmetrical driving trees. , 2010, , .		11
81	Redundant-wires-aware ECO timing and mask cost optimization. , 2010, , .		10
82	Recent research development in flip-chip routing. , 2010, , .		12
83	Three-dimensional integrated circuits (3D IC) Floorplan and Power/Ground Network Co-synthesis. , 2010, , .		41
84	Design-hierarchy aware mixed-size placement for routability optimization. , 2010, , .		19
85	Blockage-avoiding buffered clock-tree synthesis for clock latency-range and skew minimization. , 2010, , .		1
86	Predictive Formulae for OPC With Applications to Lithography-Friendly Routing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 40-50.	2.7	12
87	ECO Timing Optimization Using Spare Cells and Technology Remapping. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 697-710.	2.7	24
88	Multilayer Global Routing With Via and Wire Capacity Considerations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 685-696.	2.7	22
89	Efficient provably good OPC modeling and its applications to interconnect optimization. , 2010, , .		2
90	High-performance global routing with fast overflow reduction. , 2009, , .		38

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91	Routing for manufacturability and reliability. IEEE Circuits and Systems Magazine, 2009, 9, 20-31.	2.3	8
92	An Integer-Linear-Programming-Based Routing Algorithm for Flip-Chip Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 98-110.	2.7	42
93	A Novel Wire-Density-Driven Full-Chip Routing System for CMP Variation Control. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 193-206.	2.7	24
94	Analog Placement Based on Symmetry-Island Formulation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 791-804.	2.7	75
95	A Progressive-ILP-Based Routing Algorithm for the Synthesis of Cross-Referencing Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1295-1306.	2.7	7
96	Essential Issues in Analytical Placement Algorithms. IPSJ Transactions on System LSI Design Methodology, 2009, 2, 145-166.	0.8	35
97	A New Multilevel Framework for Large-Scale Interconnect-Driven Floorplanning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 286-294.	2.7	29
98	BioRoute: A Network-Flow-Based Routing Algorithm for the Synthesis of Digital Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1928-1941.	2.7	101
99	Metal-Density-Driven Placement for CMP Variation and Routability. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 2145-2155.	2.7	12
100	Obstacle-Avoiding Rectilinear Steiner Tree Construction Based on Spanning Graphs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 643-653.	2.7	60
101	Full-Chip Routing Considering Double-Via Insertion. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 844-857.	2.7	61
102	Effective Wire Models for X-Architecture Placement. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 654-658.	2.7	3
103	NTUplace3: An Analytical Placer for Large-Scale Mixed-Size Designs With Preplaced Blocks and Density Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1228-1240.	2.7	260
104	An Optimal Network-Flow-Based Simultaneous Diode and Jumper Insertion Algorithm for Antenna Fixing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1055-1065.	2.7	8
105	MP-Trees: A Packing-Based Macro Placement Algorithm for Modern Mixed-Size Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1621-1634.	2.7	37
106	Sensitivity-based multiple-Vt cell swapping for leakage power reduction. , 2008, , .		1
107	Constraint graph-based macro placement for modern mixed-size circuit designs. , 2008, , .		3
108	Novel wire density driven full-chip routing for CMP variation control. , 2007, , .		4

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109	Recent Research and Emerging Challenges in Physical Design for Manufacturability/Reliability. , 2007, , .		10
110	MB^{ast}-Tree: A Multilevel Floorplanner for Large-Scale Building-Module Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1430-1444.	2.7	2
111	Power/Ground Network and Floorplan Cosynthesis for Fast Design Convergence. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 693-704.	2.7	17
112	An Exact Jumper-Insertion Algorithm for Antenna Violation Avoidance/Fixing Considering Routing Obstacles. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 719-733.	2.7	5
113	Multilevel Full-Chip Routing With Testability and Yield Enhancement. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1625-1636.	2.7	10
114	An Optimal Jumper-Insertion Algorithm for Antenna Avoidance/Fixing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1818-1829.	2.7	8
115	ECO timing optimization using spare cells. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	5
116	Multilevel Full-Chip Gridless Routing With Applications to Optical-Proximity Correction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1041-1053.	2.7	18
117	An ILP algorithm for post-floorplanning voltage-island generation considering power-network planning. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	2
118	An efficient algorithm for statistical circuit optimization using lagrangian relaxation. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	0
119	Efficient multi-layer obstacle-avoiding rectilinear steiner tree construction. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	3
120	3D Video Applications and Intelligent Video Surveillance Camera and its VLSI Design. , 2007, , .		0
121	Voltage Island Aware Floorplanning for Power and Timing Optimization. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	10
122	Current Path Analysis for Electrostatic Discharge Protection. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	0
123	A High-Quality Mixed-Size Analytical Placer Considering Preplaced Blocks and Density Constraints. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	6
124	Placement of digital microfluidic biochips using the T-tree formulation. Proceedings - Design Automation Conference, 2006, , .	0.0	2
125	Modern floorplanning based on B/sup */-tree and fast simulated annealing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006, 25, 637-650.	2.7	104
126	Novel full-chip gridless routing considering double-via insertion. Proceedings - Design Automation Conference, 2006, , .	0.0	5

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127	Thermal-Driven Interconnect Optimization by Simultaneous Gate and Wire Sizing. , 2006, , .		0
128	An Optimal Simultaneous Diode/Jumper Insertion Algorithm for Antenna Fixing. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	0
129	Crosstalk- and performance-driven multilevel full-chip routing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2005, 24, 869-878.	2.7	37
130	An exact jumper insertion algorithm for antenna effect avoidance/fixing. , 2005, , .		0
131	Multilevel full-chip routing for the X-based architecture. , 2005, , .		1
132	TCG: A transitive closure graph-based representation for general floorplans. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 288-292.	3.1	46
133	Timing modeling and optimization under the transmission line model. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2004, 12, 28-41.	3.1	29
134	MR: a new framework for multilevel full-chip routing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 793-800.	2.7	44
135	Simultaneous Floorplan and Buffer-Block Optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 694-703.	2.7	8
136	TCG-S: Orthogonal Coupling of<tex>$rm P^ast$</tex>-Admissible Representations for General Floorplans. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 968-980.	2.7	42
137	Inductance Modeling for On-Chip Interconnects. Analog Integrated Circuits and Signal Processing, 2003, 35, 65-78.	1.4	5
138	Corner sequence - a P-admissible floorplan representation with a worst case linear-time packing scheme. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2003, 11, 679-686.	3.1	48
139	A fast crosstalk- and performance-driven multilevel routing system. , 2003, , .		1
140	TCG-S: orthogonal coupling of P*-admissible representations for general floorplans. , 2002, , .		2
141	Simultaneous Buffer-sizing and Wire-sizing for Clock Trees Based on Lagrangian Relaxation. VLSI Design, 2002, 15, 587-594.	0.5	4
142	An algorithm for dynamically reconfigurable FPGA placement. , 0, , .		2
143	Performance optimization by wire and buffer sizing under the transmission line model. , 0, , .		3
144	A novel framework for multilevel routing considering routability and performance. , 0, , .		0

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145	Formulae for performance optimization and their applications to interconnect-driven floorplanning. , 0, , .		0
146	Simultaneous floorplanning and buffer block planning. , 0, , .		2
147	Noise-aware buffer planning for interconnect-driven floorplanning. , 0, , .		0
148	Multilevel floorplanning/placement for large-scale modules using B*-trees. , 0, , .		0
149	A reusable methodology for non-slicing floorplanning. , 0, , .		0
150	RLC effects on worst-case switching pattern for on-chip buses. , 0, , .		9
151	Temporal floorplanning using the T-tree formulation. , 0, , .		40
152	Multilevel routing with jumper insertion for antenna avoidance. , 0, , .		0
153	Layout techniques for on-chip interconnect inductance reduction. , 0, , .		0
154	Reconfigurable Platform for Content Science Research. , 0, , .		0
155	A routing algorithm for flip-chip design. , 0, , .		5
156	Placement with symmetry constraints for analog layout design using TCG-S. , 0, , .		22
157	IMF: interconnect-driven multilevel floorplanning for large-scale building-module designs. , 0, , .		12
158	Multilevel full-chip gridless routing considering optical proximity correction. , 0, , .		5
159	IEEE standard 1500 compatible interconnect diagnosis for delay and crosstalk faults. , 0, , .		0
160	Simultaneous block and I/O buffer floorplanning for flip-chip design. , 0, , .		3
161	Inductance Extraction for General Interconnect Structures. , 0, , .		0