Hanho Lee

List of Publications by Year
in descending order

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88	735	758635 12	752256 20
papers	citations	h-index	g-index

88	88	88	427
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Efficient First Four Minimum Values Finder for NB-LDPC Decoders With Compressed Messages. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 1024-1028.	2.2	3
2	Configurable Mixed-Radix Number Theoretic Transform Architecture for Lattice-Based Cryptography. IEEE Access, 2022, 10, 12732-12741.	2.6	5
3	Low-Complexity Multi-Size Circular-Shift Network for 5G New Radio LDPC Decoders. Sensors, 2022, 22, 1792.	2.1	2
4	An Analysis of Hardware Design of MLWE-Based Public-Key Encryption and Key-Establishment Algorithms. Electronics (Switzerland), 2022, 11, 891.	1.8	2
5	Area-Time Efficient Hardware Architecture for CRYSTALS-Kyber. Applied Sciences (Switzerland), 2022, 12, 5305.	1.3	5
6	Minimal-Set Trellis Min-Max Decoder Architecture for Nonbinary LDPC Codes. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 216-220.	2.2	9
7	Low-Complexity High-Throughput QC-LDPC Decoder for 5G New Radio Wireless Communication. Electronics (Switzerland), 2021, 10, 516.	1.8	16
8	High-Efficient Nonbinary LDPC Decoder with Early Layer Decoding Schedule. , 2021, , .		1
9	Configurable Butterfly Unit Architecture for NTT/INTT in Homomorphic Encryption. , 2021, , .		4
10	High Efficiency Ring-LWE Cryptoprocessor Using Shared Arithmetic Components. Electronics (Switzerland), 2020, 9, 1075.	1.8	0
11	Efficient NewHope Cryptography Based Facial Security System on a GPU. IEEE Access, 2020, 8, 108158-108168.	2.6	15
12	High-efficiency Low-latency NTT Polynomial Multiplier for Ring-LWE Cryptography. Journal of Semiconductor Technology and Science, 2020, 20, 220-223.	0.1	1
13	Efficient k-Parallel Pipelined NTT Architecture for Post Quantum Cryptography. , 2020, , .		3
14	Efficient Check Node Unit Architecture for Non-binary Quasi-Cyclic LDPC Codes. , 2020, , .		1
15	Half-row modified two-extra-column trellis min-max decoder architecture for nonbinary LDPC codes. The Integration VLSI Journal, 2019, 69, 234-241.	1.3	1
16	Efficient QC-LDPC Encoder for 5G New Radio. Electronics (Switzerland), 2019, 8, 668.	1.8	39
17	Efficient-Scheduling Parallel Multiplier-Based Ring-LWE Cryptoprocessors. Electronics (Switzerland), 2019, 8, 413.	1.8	9
18	High-Secure Fingerprint Authentication System Using Ring-LWE Cryptography. IEEE Access, 2019, 7, 23379-23387.	2.6	22

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19	Ring-LWE Based Face Encryption and Decryption System on a GPU. , 2019, , .		3
20	Simplified Variable Node Unit Architecture for Nonbinary LDPC Decoder. , 2019, , .		0
21	Low-complexity multi-mode multi-way split-row layered LDPC decoder for gigabit wireless communications. The Integration VLSI Journal, 2019, 65, 189-200.	1.3	8
22	Basic-Set Trellis Minâ€“Max Decoder Architecture for Nonbinary LDPC Codes With High-Order Galois Fields. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 496-507.	2.1	25
23	Efficient Four-way Row-splitting Layered QC-LDPC Decoder Architecture. , 2018, , .		1
24	Low-complexity Check Node Processing for Trellis Min-max Nonbinary LDPC Decoding. , 2018, , .		0
25	Reduced-Complexity Trellis Min-Max Decoder for Non-Binary Ldpc Codes. , 2018, , .		1
26	High-Secure Low-Latency Ring-LWE Cryptography Scheme for Biomedical Images Storing and Transmitting. , 2018, , .		5
27	High-performance Ring-LWE Cryptography Scheme for Biometric Data Security. IEIE Transactions on Smart Processing and Computing, 2018, 7, 97-106.	0.3	7
28	Two-Extra-Column Trellis Minâ€“Max Decoder Architecture for Nonbinary LDPC Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1787-1791.	2.1	16
29	A delay-efficient ring-LWE cryptography architecture for biometric security. , 2017, , .		2
30	Parallel architecture for concatenated polar-CRC codes. , 2017, , .		0
31	An Area-efficient Half-row Pipelined Layered LDPC Decoder Architecture. Journal of Semiconductor Technology and Science, 2017, 17, 845-853.	0.1	4
32	High-throughput Low-complexity Mixed-radix FFT Processor using a Dual-path Shared Complex Constant Multiplier. Journal of Semiconductor Technology and Science, 2017, 17, 101-109.	0.1	5
33	Low latency check node unit architecture for nonbinary LDPC decoding. , 2016, , .		0
34	Efficient Algorithm and Architecture for Elliptic Curve Cryptographic Processor. Journal of Semiconductor Technology and Science, 2016, 16, 118-125.	0.1	18
35	Area efficient half row pipelined layered LDPC decoder for gigabit wireless communications. , 2015, , .		2
36	Parallel block-layered nonbinary QC-LDPC decoding on GPU. , 2015, , .		7

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37	High-speed low-complexity elliptic curve cryptographic processor. , 2015, , .		1
38	Efficient multi-Gb/s multi-mode LDPC decoder architecture for IEEE 802.11ad applications. The Integration VLSI Journal, 2015, 51, 21-36.	1.3	6
39	Block-Layered Decoder Architecture for Quasi-Cyclic Nonbinary LDPC Codes. Journal of Signal Processing Systems, 2015, 78, 209-222.	1.4	2
40	Multi-Gb/s multi-mode LDPC decoder architecture for IEEE 802.11ad standard. , 2014, , .		10
41	Efficient Min-Max nonbinary LDPC decoding on GPU. , 2014, , .		0
42	An efficient radix-4 Quasi-cyclic shift network for QC-LDPC decoders. IEICE Electronics Express, 2014, 11, 20130837-20130837.	0.3	3
43	Block-Circulant RS-LDPC Code: Code Construction and Efficient Decoder Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1337-1341.	2.1	11
44	A High-Speed Low-Complexity Modified ${m Radix}-2^{5}$ FFT Processor for High Rate WPAN Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 187-191.	2.1	57
45	High-performance iterative BCH decoder architecture for 100 Gb/s optical communications. , 2013, , .		1
46	Concatenated non-binary LDPC and HD-FEC codes for 100Gb/s optical transport systems. , 2012, , .		5
47	A novel method of constructing Quasi-Cyclic RS-LDPC codes for 10GBASE-T Ethernet. , 2012, , .		0
48	An ultra high-speed time-multiplexing Reed-Solomon-based FEC architecture. , 2012, , .		12
49	A High-Speed Low-Complexity Concatenated BCH Decoder Architecture for 100ÂGb/s Optical Communications. Journal of Signal Processing Systems, 2012, 66, 43-55.	1.4	15
50	A High-Speed Low-Complexity Time-Multiplexing Reed-Solomon-Based FEC Architecture for Optical Communications. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2012, E95.A, 2424-2429.	0.2	0
51	High-throughput variable-length Reed-Solomon decoder for high-rate WPAN applications. , 2011, , .		2
52	Low-complexity filter and interpolator design for ATSC DTV systems. , 2011, , .		0
53	A high-speed low-complexity modified radix-2⁵ FFT processor for gigabit WPAN applications. , 2011, , .		22
54	High-Throughput Low-Complexity Four-Parallel Reed-Solomon Decoder Architecture for High-Rate WPAN Systems. IEICE Transactions on Communications, 2011, E94-B, 1332-1338.	0.4	3

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55	Low Complexity Filter Architecture for ATSC Terrestrial Broadcasting DTV Systems. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2011, E94-A, 937-945.	0.2	0
56	A Reduced-Complexity Architecture for LDPC Layered Decoding Schemes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1099-1103.	2.1	40
57	A high-throughput LDPC decoder architecture for high-rate WPAN systems. , 2011, , .		0
58	An area-efficient truncated inversionless Berlekamp-Massey architecture for Reed-Solomon decoders. , 2011, , .		8
59	Low-Complexity Multi-Mode Memory-Based FFT Processor for DVB-T2 Applications. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2011, E94-A, 2376-2383.	0.2	2
60	A high-performance concatenated BCH code and its hardware architecture for 100 Gb/s long-haul optical communications. , 2010, , .		12
61	Low-cost variable-length FFT processor for DVB-T/H applications. , 2010, , .		2
62	100GB/S two-iteration concatenated BCH decoder architecture for optical communications. , 2010, , .		3
63	High-Speed Two-Parallel Concatenated BCH-Based Super-FEC Architecture for Optical Communications. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2010, E93-A, 769-777.	0.2	5
64	High-speed low-complexity three-parallel reed-solomon decoder for 6-Gbps mmWave WPAN systems. , 2009, , .		2
65	High-speed low-complexity Reed-Solomon decoder using pipelined Berlekamp-Massey algorithm. , 2009, , .		15
66	Low-complexity folded FIR filter architecture for ATSC DTV tuner. , 2009, , .		7
67	Two-parallel concatenated BCH super-FEC architecture for 100-GB/S optical communications. , 2009, , .		3
68	A power-aware variable-precision multiply-accumulate unit. , 2009, , .		2
69	Adaptive quantization in min-sum based irregular LDPC decoder. , 2008, , .		7
70	A high-speed four-parallel radix-2⁴ FFT/IFFT processor for UWB applications. , 2008, , .		33
71	A Discrepancy-Computationless RiBM algorithm and its architecture for BCH decoders. , 2008, , .		5
72	Flexible LDPC decoder architecture for high-throughput applications. , 2008, , .		9

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73	Ubiquitous evolvable hardware system for heart disease diagnosis applications. International Journal of Electronics, 2008, 95, 637-651.	0.9	2
74	A high performance four-parallel 128/64-point radix-2⁴ FFT/IFFT processor for MIMO-OFDM systems. , 2008, , .		10
75	100-Gb/s three-parallel Reed-Solomon based foward error correction architecture for optical communications. , 2008, , .		8
76	Two bit-level pipelined viterbi decoder for high-performance UWB applications. , 2008, , .		0
77	40-Gb/s two-parallel Reed-Solomon based Forward Error Correction architecture for optical communications. , 2008, , .		1
78	Two-parallel Reed-Solomon based FEC architecture for optical communications. IEICE Electronics Express, 2008, 5, 374-380.	0.3	24
79	A High-Speed Pipelined Degree-Computationless Modified Euclidean Algorithm Architecture for Reed-Solomon Decoders. , 2007, , .		21
80	A Partial Self-Reconfigurable Adaptive FIR Filter System. Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on, 2007, , .	0.0	5
81	A high-speed low-complexity two-parallel radix-2⁴ FFT/IFFT processor for UWB applications. , 2007, , .		5
82	An Reconfigurable FIR Filter Design on a Partial Reconfiguration Platform. , 2006, , .		12
83	A high-speed low-complexity Reed-Solomon decoder for optical communications. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2005, 52, 461-465.	2.3	51
84	VLSI DESIGN OF DIGIT-SERIAL FPGA ARCHITECTURE. Journal of Circuits, Systems and Computers, 2004, 13, 17-52.	1.0	0
85	A power-aware scalable pipelined booth multiplier. , 0, , .		29
86	An Ultra High-Speed Reed-Solomon Decoder. , 0, , .		1
87	A Reconfigurable FIR Filter Design Using Dynamic Partial Reconfiguration. , 0, , .		9
88	A high-speed, low-complexity radix-2/sup 4/ FFT processor for MB-OFDM UWB systems. , 0, , .		10