Lieven Eeckhout

List of Publications by Year
in descending order

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51 papers	2,069 citations	1040056 9 h-index	477307 29 g-index
51 all docs	51 docs citations	51 times ranked	1140 citing authors

#	Article	IF	Citations
1	Sniper. , 2011, , .		577
2	System-Level Performance Metrics for Multiprogram Workloads. IEEE Micro, 2008, 28, 42-53.	1.8	338
3	An Evaluation of High-Level Mechanistic Core Models. Transactions on Architecture and Code Optimization, 2014, 11, 1-25.	2.0	231
4	A mechanistic performance model for superscalar out-of-order processors. ACM Transactions on Computer Systems, 2009, 27, 1-37.	0.8	191
5	Microarchitecture-Independent Workload Characterization. IEEE Micro, 2007, 27, 63-72.	1.8	153
6	Performance prediction based on inherent program similarity. , 2006, , .		114
7	Chip Multiprocessor Design Space Exploration through Statistical Simulation. IEEE Transactions on Computers, 2009, 58, 1668-1681.	3.4	52
8	Probabilistic job symbiosis modeling for SMT processor scheduling. , 2010, , .		52
9	Sampled simulation of multi-threaded applications. , 2013, , .		41
10	Using cycle stacks to understand scaling bottlenecks in multi-threaded workloads. , 2011, , .		31
11	Micro-architecture independent analytical processor performance and power modeling. , 2015, , .		27
12	Analytical Processor Performance and Power Modeling using Micro-Architecture Independent Characteristics. IEEE Transactions on Computers, 2016, , 1-1.	3.4	27
13	Application Clustering Policies to Address System Fairness with Intelâ€™s Cache Allocation Technology. , 2017, , .		23
14	The benefit of SMT in the multi-core era. , 2014, , .		18
15	A low-cost conflict-free NoC for GPGPUs. , 2016, , .		15
16	A heterogeneous low-cost and low-latency Ring-Chain network for GPGPUs. , 2016, , .		13
17	GDP: Using Dataflow Properties to Accurately Estimate Interference-Free Performance at Runtime. , 2018, , .		13
18	Optimizing Soft Error Reliability Through Scheduling on Heterogeneous Multicore Processors. IEEE Transactions on Computers, 2018, 67, 830-846.	3.4	13

#	Article	IF	Citations
19	Precise Runahead Execution. , 2020, , .		12
20	MIA: Metric Importance Analysis for Big Data Workload Characterization. IEEE Transactions on Parallel and Distributed Systems, 2018, 29, 1371-1384.	5.6	11
21	Ranking commercial machines through data transposition. , 2011, , .		10
22	Modeling Superscalar Processor Memory-Level Parallelism. IEEE Computer Architecture Letters, 2018, 17, 9-12.	1.5	10
23	RPPM: Rapid Performance Prediction of Multithreaded Applications on Multicore Hardware. IEEE Computer Architecture Letters, 2018, 17, 183-186.	1.5	10
24	Automated Full-System Power Characterization. IEEE Micro, 2011, 31, 46-59.	1.8	8
25	Shared resource aware scheduling on power-constrained tiled many-core processors. Journal of Parallel and Distributed Computing, 2017, 100, 30-41.	4.1	8
26	SZTS: A Novel Big Data Transportation System Benchmark Suite. , 2015, , .		7
27	SMA: A Self-Monitored Adaptive Cache Warm-Up Scheme for Microprocessor Simulation. International Journal of Parallel Programming, 2005, 33, 561-581.	1.5	6
28	HeteroCore GPU to Exploit TLP-Resource Diversity. IEEE Transactions on Parallel and Distributed Systems, 2019, 30, 93-106.	5.6	6
29	Middleware benchmarking: approaches, results, experiences. Concurrency Computation Practice and Experience, 2005, 17, 1799-1805.	2.2	5
30	CD-Xbar: A Converge-Diverge Crossbar Network for High-Performance GPUs. IEEE Transactions on Computers, 2019, 68, 1283-1296.	3.4	5
31	Selective Replication in Memory-Side GPU Caches. , 2020, , .		5
32	64-bit versus 32-bit Virtual Machines for Java. Software - Practice and Experience, 2006, 36, 1-26.	3.6	4
33	Improving IBM POWER8 Performance Through Symbiotic Job Scheduling. IEEE Transactions on Parallel and Distributed Systems, 2017, 28, 2838-2851.	5.6	4
34	Modeling Emerging Memory-Divergent GPU Applications. IEEE Computer Architecture Letters, 2019, 18, 95-98.	1.5	4
35	Intra-Cluster Coalescing and Distributed-Block Scheduling to Reduce GPU NoC Pressure. IEEE Transactions on Computers, 2019, 68, 1064-1076.	3.4	4
36	Thread Isolation to Improve Symbiotic Scheduling on SMT Multicore Processors. IEEE Transactions on Parallel and Distributed Systems, 2020, 31, 359-373.	5.6	4

#	Article	IF	Citations
37	Per-Thread Cycle Accounting. IEEE Micro, 2010, 30, 71-80.	1.8	3
38	Precise Runahead Execution. IEEE Computer Architecture Letters, 2019, 18, 71-74.	1.5	3
39	Vector Runahead. , 2021, , .		3
40	Linear Branch Entropy: Characterizing and Optimizing Branch Behavior in a Micro-Architecture Independent Way. IEEE Transactions on Computers, 2017, 66, 458-472.	3.4	2
41	Evaluation of the Gini-index for Studying Branch Prediction Features. AIP Conference Proceedings, 2004, , .	0.4	1
42	An Analysis of Program Phase Behavior and its Predictability. AIP Conference Proceedings, 2006, , .	0.4	1
43	Shorter On-Line Warmup for Sampled Simulation of Multi-threaded Applications. , 2015, , .		1
44	Hot Chips in an Increasingly Diverse Microprocessor Landscape. IEEE Micro, 2015, 35, 2-3.	1.8	1
45	Scale-Model Simulation. IEEE Computer Architecture Letters, 2021, 20, 175-178.	1.5	1
46	Vector Runahead for Indirect Memory Accesses. IEEE Micro, 2022, 42, 116-123.	1.8	1
47	Predictive Learning in Two-Way Datasets. , 2014, , 61-68.		0
48	Looking Forward to Upcoming Themes. IEEE Micro, 2017, 37, 4-5.	1.8	0
49	VMT: Virtualized Multi-Threading for Accelerating Graph Workloads on Commodity Processors. IEEE Transactions on Computers, 2022, 71, 1386-1398.	3.4	0
50	Reliability-Aware Runahead. , 2022, , .		0
51	Scale-Model Architectural Simulation. , 2022, , .		0