James E Stine

List of Publications by Year
in descending order

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55 papers	705 citations	2258059 3 h-index	2053705 5 g-index
55 all docs	55 docs citations	55 times ranked	445 citing authors

#	Article	IF	Citations
1	FreePDK: An Open-Source Variation-Aware Design Kit. , 2007, , .		296
2	The Symmetric Table Addition Method for Accurate Function Approximation. Journal of Signal Processing Systems, 1999, 21, 167-177.	1.0	99
3	OpenRAM: an open-source memory compiler. , 2016, , .		94
4	Compressor trees for decimal partial product reduction. , 2008, , .		22
5	A 64 kB Approximate SRAM Architecture for Low-Power Video Applications. IEEE Embedded Systems Letters, 2018, 10, 10-13.	1.9	22
6	FreePDK v2.0: Transitioning VLSI education towards nanometer variation-aware designs. , 2009, , .		16
7	Digital Computer Arithmetic Datapath Design Using Verilog HDL. , 2004, , .		15
8	Additional optimizations for parallel squarer units. , 2014, , .		13
9	Optimized Linear, Quadratic and Cubic Interpolators for Elementary Function Hardware Implementations. Electronics (Switzerland), 2016, 5, 17.	3.1	12
10	A 64 kb differential single-port 12T SRAM design with a bit-interleaving scheme for low-voltage operation in 32 nm SOI CMOS. , 2016, , .		10
11	Parallel Prefix Ling Structures for Modulo 2^n-1 Addition. , 2009, , .		9
12	Partial Product Reduction for Parallel Cubing. , 2007, , .		8
13	Experiments with High Speed Parallel Cubing Units. , 2014, , .		7
14	Multi Replica Bitline Delay Technique for Variation Tolerant Timing of SRAM Sense Amplifiers. , 2015, , .		7
15	A high performance multi-port SRAM for low voltage shared memory systems in 32 nm CMOS. , 2017, , .		7
16	Sustainable IC design and fabrication. , 2017, , .		7
17	Optimized low-power elementary function approximation for Chebyshev series approximations. , 2012, , .		5
18	A Comprehensive Exploration of the Parallel Prefix Adder Tree Space. , 2021, , .		5

#	Article	IF	Citations
19	A Novel Single/Double Precision Normalized IEEE 754 Floating-Point Adder/Subtracter. , 2019, , .		4
20	Fast and Area-Efficient SRAM Word-Line Optimization. , 2019, , .		4
21	Intrinsic Compiler Support for Interval Arithmetic. Numerical Algorithms, 2004, 37, 13-20.	1.9	3
22	Enhancing parallel-prefix structures using carry-save notation. , 2008, , .		3
23	Decimal partial product generation architectures. , 2008, , .		3
24	An IEEE 754 double-precision floating-point multiplier for denormalized and normalized floating-point numbers. , 2015, , .		3
25	WIP. Open-source standard cell characterization process flow on 45 nm (FreePDK45), 0.18 Âµm, 0.25 Âµm, 0.35 Âµm and 0.5 Âµm. , 2017, , .		3
26	A combined IEEE half and single precision floating point multipliers for deep learning. , 2017, , .		3
27	Constant-based truncated cubing architectures. , 2017, , .		3
28	Low-Area Memoryless optimized Soft-Decision Viterbi Decoder with Dedicated Paralell Squaring Architecture. , 2018, , .		3
29	A Multi-Mode Low-Energy Binary Adder. , 2006, , .		2
30	Optimized cubic chebyshev interpolator for elementary function hardware implementations. , 2014, , .		2
31	A differential single-port 8T SRAM bitcell for variability tolerance and low voltage operation. , 2015, , .		2
32	A Novel Rounding Algorithm for a High Performance IEEE 754 Double-Precision Floating-Point Multiplier. , 2020, , .		2
33	Experiments for Decimal Floating-Point Division by Recurrence. , 2006, , .		1
34	Pipelining high-radix SRT division algorithms. Midwest Symposium on Circuits and Systems, 2007, , .	1.0	1
35	A recursive-divide architecture for multiplication and division. , 2011, , .		1
36	Elementary function approximation using optimized most significant bits of Chebyshev coefficients and truncated multipliers. , 2012, , .		1

#	Article	IF	Citations
37	Revisiting redundant Booth with bias multipliers. , 2015, , .		1
38	Clarifications and Optimizations on Rounding for IEEE-compliant Floating-Point Multiplication. , 2018, , .		1
39	Using Carry Increment Adders to Enhance Energy Savings with Spanning-Tree Adder Structures. , 2019, , .		1
40	A Low-Power Recurrence-Based Radix 4 Divider Using Signed-Digit Addition. , 2019, , .		1
41	Conditional Estimation of Residuals with Prescaling for Use in Low-Energy Division Units. , 2019, , .		1
42	An Efficient Implementation of Radix-4 Integer Division Using Scaling. , 2020, , .		1
43	A Reconfigurable Architecture for Improvement and Optimization of Advanced Encryption Standard Hardware. , 2021, , .		1
44	A 64-bit Decimal Floating-Point Comparator. , 2006, , .		0
45	Low Power and High Speed Addition Strategies for VLSI. , 2006, , .		0
46	Single-ended half-swing low-power SRAM design. , 2008, , .		0
47	Enhancing the Unified Logical Effort algorithm for branching and load distribution. , 2014, , .		0
48	Optimized multipartite table methods for elementary function computation. , 2016, , .		0
49	A 64 kb multi-threshold SRAM array with novel differential 8T bitcell in 32 nm SOI CMOS technology. , 2016, , .		0
50	A Methodology for Low-Power Approximate Embedded SRAM Within Multimedia Applications. , 2018, , .		0
51	An Emphasis on Memory and Processor Interactions in Undergraduate Computer Architecture Education. , 2019, , .		0
52	A Well-Equipped Implementation: Normal/Denormalized Half/Single/Double Precision IEEE 754 Floating-Point Adder/Subtracter. , 2019, , .		0
53	An Improved Hardware Architecture for modulo without Multiplication. , 2020, , .		0
54	A Ling-Enhanced Adder for IEEE-compliant Floating-Point Multiplication. , 2020, , .		0

#	Article	IF	Citations
55	An Architecture for Improving Variable Radix Real and Complex Division Using Recurrence Division. , 2020, , .		0