Swaroop Ghosh

List of Publications by Year
in descending order

84 papers	976 citations	623188 14 h-index	713013 21 g-index
84 all docs	84 docs citations	84 times ranked	640 citing authors

#	Article	IF	Citations
1	Spintronics and Security: Prospects, Vulnerabilities, Attack Models, and Preventions. Proceedings of the IEEE, 2016, 104, 1864-1893.	16.4	52
2	How Secure Are Printed Circuit Boards Against Trojan Attacks?. IEEE Design and Test, 2015, 32, 7-16.	1.1	51
3	Sensitivity based Error Resilient Techniques for Energy Efficient Deep Neural Network Accelerators. , 2019, , .		31
4	Impact of Process-Variations in STTRAM and Adaptive Boosting for Robustness. , 2015, , .		30
5	Self-correcting STTRAM under magnetic field attacks. , 2015, , .		30
6	A novel threshold voltage defined switch for circuit camouflaging. , 2016, , .		30
7	CSRO-Based Reconfigurable True Random Number Generator Using RRAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2661-2670.	2.1	29
8	MTJ-Based State Retentive Flip-Flop With Enhanced-Scan Capability to Sustain Sudden Power Failure. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2062-2068.	3.5	27
9	Quantum Generative Models for Small Molecule Drug Discovery. IEEE Transactions on Quantum Engineering, 2021, 2, 1-8.	2.9	27
10	Security and privacy threats to on-chip non-volatile memories and countermeasures. , 2016, , .		23
11	Quantum PUF for Security and Trust in Quantum Computing. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 333-342.	2.7	23
12	A 1 Gb 2 GHz 128 GB/s Bandwidth Embedded DRAM in 22 nm Tri-Gate CMOS Technology. IEEE Journal of Solid-State Circuits, 2015, 50, 150-157.	3.5	22
13	Experimental Characterization, Modeling, and Analysis of Crosstalk in a Quantum Computer. IEEE Transactions on Quantum Engineering, 2020, 1, 1-6.	2.9	22
14	Domain Wall Memory-Layout, Circuit and Synergistic Systems. IEEE Nanotechnology Magazine, 2015, 14, 282-291.	1.1	21
15	Side-Channel Attack on STTRAM Based Cache for Cryptographic Application. , 2017, , .		20
16	MUQUT: Multi-Constraint Quantum Circuit Mapping on NISQ Computers: Invited Paper. , 2019, , .		20
17	Design, Analysis and Application of Embedded Resistive RAM Based Strong Arbiter PUF. IEEE Transactions on Dependable and Secure Computing, 2020, 17, 1232-1242.	3.7	20
18	Domain Wall Magnets for Embedded Memory and Hardware Security. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2015, 5, 40-50.	2.7	19

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19	Data privacy in non-volatile cache: Challenges, attack models and solutions. , 2016, , .		16
20	Fault injection attacks on emerging non-volatile memory and countermeasures. , 2018, , .		16
21	Sensitivity-Based Error Resilient Techniques With Heterogeneous Multiplyâ€“Accumulate Unit for Voltage Scalable Deep Neural Network Accelerators. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 520-531.	2.7	16
22	A Family of Compact Non-Volatile Flip-Flops With Ferroelectric FET. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4219-4229.	3.5	16
23	ROBIN: Monolithic-3D SRAM for Enhanced Robustness with In-Memory Computation Support. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2533-2545.	3.5	16
24	Retention time optimization for eDRAM in 22nm tri-gate CMOS technology. , 2013, , .		15
25	Domain Wall Memory based Convolutional Neural Networks for Bit-width Extendability and Energy-Efficiency. , 2016, , .		15
26	Analysis of crosstalk in NISQ devices and security implications in multi-programming regime. , 2020, , .		15
27	Side channel attacks on STTRAM and low-overhead countermeasures. , 2016, , .		14
28	Exploiting Serial Access and Asymmetric Read/Write of Domain Wall Memory for Area and Energy-Efficient Digital Signal Processor Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 91-102.	3.5	14
29	Spintronic PUFs for Security, Trust, and Authentication. ACM Journal on Emerging Technologies in Computing Systems, 2017, 13, 1-15.	1.8	13
30	Design methodologies for high density domain wall memory. , 2013, , .		12
31	Hardware Assisted Buffer Protection Mechanisms for Embedded RISC-V. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4453-4465.	1.9	12
32	Cache-Out: Leaking Cache Memory Using Hardware Trojan. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1461-1470.	2.1	12
33	Retention Testing Methodology for STTRAM. IEEE Design and Test, 2016, 33, 7-15.	1.1	11
34	Information Leakage Attacks on Emerging Non-Volatile Memory and Countermeasures. , 2018, , .		11
35	Addressing Temporal Variations in Qubit Quality Metrics for Parameterized Quantum Circuits. , 2019, , .		11
36	An Efficient Circuit Compilation Flow for Quantum Approximate Optimization Algorithm. , 2020, , .		11

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37	HarTBleed: Using Hardware Trojans for Data Leakage Exploits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 968-979.	2.1	11
38	Quantum-Classical Hybrid Machine Learning for Image Classification (ICCAD Special Session Paper). , 2021, , .		11
39	Comprehensive Study of Security and Privacy of Emerging Non-Volatile Memories. Journal of Low Power Electronics and Applications, 2021, 11, 36.	1.3	10
40	A strong arbiter PUF using resistive RAM within 1T-1R memory architecture. , 2016, , .		9
41	Replacing eFlash with STTRAM in IoTs: Security Challenges and Solutions. Journal of Hardware and Systems Security, 2017, 1, 328-339.	0.8	9
42	How Multi-Threshold Designs Can Protect Analog IPs. , 2018, , .		9
43	A Perspective on Test Methodologies for Supervised Machine Learning Accelerators. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 562-569.	2.7	9
44	SHINE: A Novel SHA-3 Implementation Using ReRAM-based In-Memory Computing. , 2019, , .		9
45	A Survey and Tutorial on Security and Resilience of Quantum Computing. , 2021, , .		9
46	Adaptive Write and Shift Current Modulation for Process Variation Tolerance in Domain Wall Caches. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 944-953.	2.1	8
47	Threshold Defined Camouflaged Gates in 65nm Technology for Reverse Engineering Protection. , 2018, , .		8
48	Novel magnetic burn-in for retention testing of STTRAM. , 2017, , .		7
49	Analysis of Row Hammer Attack on STTRAM. , 2018, , .		7
50	Spintronics for associative computation and hardware security. , 2015, , .		6
51	Investigation of magnetic field attacks on commercial Magneto-Resistive Random Access Memory. , 2017, , .		6
52	Preventing Reverse Engineering using threshold voltage defined multi-input camouflaged gates. , 2017, , .		6
53	Dynamic Computing in Memory (DCIM) in Resistive Crossbar Arrays. , 2018, , .		6
54	Novel Magnetic Burn-In for Retention and Magnetic Tolerance Testing of STTRAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1508-1517.	2.1	6

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55	ReLOPE: Resistive RAM-Based Linear First-Order Partial Differential Equation Solver. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 237-241.	2.1	6
56	Comprehensive Study of Side-Channel Attack on Emerging Non-Volatile Memories. Journal of Low Power Electronics and Applications, 2021, 11, 38.	1.3	6
57	FPCAS: In-Memory Floating Point Computations for Autonomous Systems. , 2019, , .		5
58	Domain Wall Memory-Based Design of Deep Neural Network Convolutional Layers. IEEE Access, 2020, 8, 19783-19798.	2.6	5
59	Scalable Variational Quantum Circuits for Autoencoder-based Drug Discovery. , 2022, , .		5
60	Modeling of Retention Time for High-Speed Embedded Dynamic Random Access Memories. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 2596-2604.	3.5	4
61	VFAB: A Novel 2-Stage STTRAM Sensing Using Voltage Feedback and Boosting. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1919-1928.	3.5	4
62	Design Space Exploration for Selector Diode-STTRAM Crossbar Arrays. IEEE Transactions on Magnetics, 2018, 54, 1-5.	1.2	4
63	Cache Bypassing and Checkpointing to Circumvent Data Security Attacks on STTRAM. IEEE Transactions on Emerging Topics in Computing, 2019, 7, 262-270.	3.2	4
64	Threshold-Defined Logic and Interconnect for Protection Against Reverse Engineering. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 308-320.	1.9	4
65	SecNVM: Power Side-Channel Elimination Using On-Chip Capacitors for Highly Secure Emerging NVM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1518-1528.	2.1	4
66	Split Compilation for Security of Quantum Circuits. , 2021, , .		4
67	Guest Editorial Emerging Memoriesâ€"Technology, Architecture and Applications (First Issue). IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2016, 6, 105-108.	2.7	3
68	Methodologies to exploit ATPG tools for de-camouflaging. , 2017, , .		3
69	Novel application of spintronics in computing, sensing, storage and cybersecurity. , 2018, , .		3
70	SCARE: Side Channel Attack on In-Memory Computing for Reverse Engineering. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 2040-2051.	2.1	3
71	Shuttle-Exploiting Attacks and Their Defenses in Trapped-Ion Quantum Computers. IEEE Access, 2022, 10, 2686-2699.	2.6	3
72	Test of Supply Noise for Emerging Non-Volatile Memory. , 2018, , .		2

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73	Reconfigurable and Dense Analog Circuit Design Using Two Terminal Resistive Memory. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 1596-1608.	3.2	2
74	Test Methodologies and Test-Time Compression for Emerging Non-Volatile Memory. IEEE Transactions on Reliability, 2020, 69, 1387-1397.	3.5	2
75	A Morphable Physically Unclonable Function and True Random Number Generator Using a Commercial Magnetic Memory. Journal of Low Power Electronics and Applications, 2021, 11, 5.	1.3	2
76	Assuring Security and Reliability of Emerging Non-Volatile Memories. , 2020, , .		2
77	Security Aspects of Quantum Machine Learning: Opportunities, Threats and Defenses. , 2022, , .		2
78	Energy centric model of SRAM write operation for improved energy and error rates. , 2013, , .		1
79	iMACE: In-Memory Acceleration of Classic McEliece Encoder. , 2019, , .		1
80	FAuto: An Efficient GMM-HMM FPGA Implementation for Behavior Estimation in Autonomous Systems. , 2020, , .		1
81	Recent Advances in Emerging Technology-based Security Primitives, Attacks and Mitigation. , 2020, , .		1
82	Addressing Resiliency of In-Memory Floating Point Computation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1172-1183.	2.1	1
83	Guest Editorial Emerging Memoriesâ€"Technology, Architecture and Applications (Second Issue). IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2016, 6, 261-264.	2.7	0
84	Meeting the Conflicting Goals of Low-Power and Resiliency Using Emerging Memories : (Invited Paper). , 2019, , .		0