Fady Abouzeid

List of Publications by Year
in descending order

34	352	1163117 8	1125743 13
papers	citations	h-index	g-index

34	34	34	337
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A 460 MHz at 397 mV, 2.6 GHz at 1.3 V, 32 bits VLIW DSP Embedding F MAX Tracking. IEEE Journal of Solid-State Circuits, 2015, 50, 125-136.	5.4	42
2	A 225 Î¼m ^{2} Probe Single-Point Calibration Digital Temperature Sensor Using Body-Bias Adjustment in 28 nm FD-SOI CMOS. IEEE Solid-State Circuits Letters, 2018, 1, 14-17.	2.0	30
3	A 460MHz at 397mV, 2.6GHz at 1.3V, 32b VLIW DSP, embedding F_{MAX} tracking. , 2014, , .		29
4	A 2.7 pJ/cycle 16 MHz, 0.7 <inline-formula> <tex-math notation="LaTeX">$muext{W}$ </tex-math> </inline-formula> Deep Sleep Power ARM Cortex-M0+ Core SoC in 28 nm FD-SOI. IEEE Journal of Solid-State Circuits, 2018, 53, 2088-2100.	5.4	28
5	8.4 A 0.33V/-40°C process/temperature closed-loop compensation SoC embedding all-digital clock multiplier and DC-DC converter exploiting FDSOI 28nm back-gate biasing. , 2015, , .		23
6	Scalable 0.35 V to 1.2 V SRAM Bitcell Design From 65 nm CMOS to 28 nm FDSOI. IEEE Journal of Solid-State Circuits, 2014, 49, 1499-1505.	5.4	19
7	193 MOPS/mW @ 162 MOPS, 0.32V to 1.15V voltage range multi-core accelerator for energy efficient parallel and sequential digital processing. , 2016, , .		18
8	Sub-threshold 10T SRAM bit cell with read/write XY selection. Solid-State Electronics, 2015, 106, 1-11.	1.4	16
9	A 45nm CMOS 0.35v-optimized standard cell library for ultra-low power applications. , 2009, , .		13
10	28nm CMOS, energy efficient and variability tolerant, 350mV-to-1.0V, 10MHz/700MHz, 252bits frame error-decoder. , 2012, , .		12
11	Process Variability Effect on Soft Error Rate by Characterization of Large Number of Samples. IEEE Transactions on Nuclear Science, 2012, 59, 2914-2919.	2.0	10
12	Experimental Soft Error Rate of Several Flip-Flop Designs Representative of Production Chip in 32Ânm CMOS Technology. IEEE Transactions on Nuclear Science, 2013, 60, 4226-4231.	2.0	10
13	28nm FD-SOI technology and design platform for sub-10pJ/cycle and SER-immune 32bits processors. , 2015, , .		9
14	A 1.1-pJ/cycle, 20-MHz, 0.42-V Temperature Compensated ARM Cortex-M0+ SoC With Adaptive Self Body-Biasing in FD-SOI. IEEE Solid-State Circuits Letters, 2018, 1, 174-177.	2.0	9
15	A 65nm SRAM achieving 250mV retention and 350mV, 1MHz, 55fJ/bit access energy, with bit-interleaved radiation Soft Error tolerance. , 2012, , .		8
16	On-Chip Total Ionizing Dose Digital Monitor in Fully Depleted SOI Technologies. IEEE Transactions on Nuclear Science, 2020, 67, 1326-1331.	2.0	8
17	A 2.7pJ/cycle 16MHz SoC with 4.3nW power-off ARM Cortex-M0+ core in 28nm FD-SOI. , 2017, , .		7
18	Single-Event Transient Space Characterizations in 28-nm UTBB SOI Technologies and Below. IEEE Transactions on Nuclear Science, 2021, 68, 21-26.	2.0	7

#	Article	IF	Citations
19	Radiation-Hardened Cortex-R4F System-on-Chip Prototype With Total Ionizing Dose Dynamic Compensation in 28-nm FD-SOI. IEEE Transactions on Nuclear Science, 2021, 68, 1040-1044.	2.0	7
20	40nm CMOS 0.35V-Optimized Standard Cell Libraries for Ultra-Low Power Applications. ACM Transactions on Design Automation of Electronic Systems, 2011, 16, 1-17.	2.6	6
21	A 0.32V, 55fJ per bit access energy, CMOS 65nm bit-interleaved SRAM with radiation Soft Error tolerance. , 2012, , .		6
22	Space radiation and reliability qualifications on 65nm CMOS 600MHz microprocessors. , 2013, , .		6
23	Q-Learning-based Adaptive Power Management for IoT System-on-Chips with Embedded Power States. , 2018, , .		6
24	Influence of Supply Voltage and Body Biasing on Single-Event Upsets and Single-Event Transients in UTBB FD-SOI. IEEE Transactions on Nuclear Science, 2021, 68, 850-856.	2.0	5
25	A 40nm CMOS, 1.27nJ, 330mV, 600kHz, Bose Chaudhuri Hocquenghem 252 bits frame decoder. , 2010, , .		4
26	A 240mV 1MHz, 340mV 10MHz, 40nm CMOS, 252 bits frame decoder using ultra-low voltage circuit design platform. , 2011, , .		4
27	Investigating the single-event-transient sensitivity of 65 nm clock trees with heavy ion irradiation and Monte-Carlo simulation. , 2016, , .		3
28	30% static power improvement on ARM CortexÂ®-A53 using static biasing-anticipation. , 2016, , .		3
29	0.42-to-1.20V read assist circuit for SRAMs in CMOS 65nm. , 2013, , .		2
30	Scalable 0.35V to 1.2V SRAM bitcell design from 65nm CMOS to 28nm FDSOI. , 2013, , .		2
31	Reduction of IPs energy consumption with ultra-low voltage supply. , 2014, , .		0
32	A 0.40pJ/cycle 981 Î¼m2 voltage scalable digital frequency generator for SoC clocking. , 2017, , .		0
33	Body-Bias Calibration Based Temperature Sensor. Integrated Circuits and Systems, 2020, , 243-261.	0.2	0
34	CLASS: on-Chip Lightweight Accurate SEU/SET event claSSifier. , 2019, , .		0