Michael L Scott

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/1750260/publications.pdf

Version: 2024-02-01

95 papers	4,724 citations	361413 20 h-index	233421 45 g-index
99 all docs	99 docs citations	99 times ranked	1156 citing authors

#	Article	IF	Citations
1	Algorithms for scalable synchronization on shared-memory multiprocessors. ACM Transactions on Computer Systems, 1991, 9, 21-65.	0.8	986
2	Simple, fast, and practical non-blocking and blocking concurrent queue algorithms. , 1996, , .		503
3	Advanced contention management for dynamic software transactional memory. , 2005, , .		296
4	NOrec. , 2010, , .		177
5	Nonblocking Algorithms and Preemption-Safe Locking on Multiprogrammed Shared Memory Multiprocessors. Journal of Parallel and Distributed Computing, 1998, 51, 1-26.	4.1	149
6	Dynamically tuning processor resources with adaptive processing. Computer, 2003, 36, 49-58.	1.1	127
7	Flexible Decoupled Transactional Memory Support. , 2008, , .		104
8	First-class user-level threads. , 1991, , .		95
9	Synchronization without contention. , 1991, , .		90
10	Dynamic frequency and voltage scaling for a multiple-clock-domain microprocessor. IEEE Micro, 2003, 23, 62-68.	1.8	87
11	Privatization techniques for software transactional memory. , 2007, , .		85
12	Linearizability of Persistent Memory Objects Under a Full-System-Crash Failure Model. Lecture Notes in Computer Science, 2016, , 313-327.	1.3	79
13	Conflict Detection and Validation Strategies for Software Transactional Memory. Lecture Notes in Computer Science, 2006, , 179-193.	1.3	73
14	Hybrid NOrec. , 2011, , .		71
15	An integrated hardware-software approach to flexible transactional memory. , 2007, , .		69
16	A comprehensive strategy for contention management in software transactional memory. , 2009, , .		69
17	NUMA policies and their relation to memory architecture. , 1991, , .		68
18	Scalable reader-writer synchronization for shared-memory multiprocessors. , 1991, , .		68

#	Article	IF	Citations
19	Scheduler-conscious synchronization. ACM Transactions on Computer Systems, 1997, 15, 3-40.	0.8	66
20	Profile-based dynamic voltage and frequency scaling for a multiple clock domain microprocessor. , 2003, , .		65
21	Design tradeoffs in modern software transactional memory systems. , 2004, , .		59
22	iDO: Compiler-Directed Failure Atomicity for Nonvolatile Memory. , 2018, , .		58
23	An efficient algorithm for concurrent priority queue heaps. Information Processing Letters, 1996, 60, 151-157.	0.6	49
24	Scalable queue-based spin locks with timeout. , 2001, , .		44
25	NOrec. ACM SIGPLAN Notices, 2010, 45, 67-78.	0.2	44
26	Delaunay Triangulation with Transactions and Barriers. , 2007, , .		43
27	Implementing and Exploiting Inevitability in Software Transactional Memory. , 2008, , .		41
28	Disengaged scheduling for fair, protected access to fast computational accelerators. , 2014, , .		40
29	Scalable Techniques for Transparent Privatization in Software Transactional Memory. , 2008, , .		38
30	Scalable reader-writer synchronization for shared-memory multiprocessors. ACM SIGPLAN Notices, 1991, 26, 106-113.	0.2	36
31	Fast, contention-free combining tree barriers for shared-memory multiprocessors. International Journal of Parallel Programming, 1994, 22, 449-481.	1.5	34
32	Non-blocking timeout in scalable queue-based spin locks. , 2002, , .		34
33	Ordering-Based Semantics for Software Transactional Memory. Lecture Notes in Computer Science, 2008, , 275-294.	1.3	31
34	Preemption Adaptivity in Time-Published Queue-Based Spin Locks. Lecture Notes in Computer Science, 2005, , 7-18.	1.3	30
35	Flexible Decoupled Transactional Memory Support. Computer Architecture News, 2008, 36, 139-150.	2.5	29
36	A comprehensive strategy for contention management in software transactional memory. ACM SIGPLAN Notices, 2009, 44, 141-150.	0.2	28

#	Article	IF	Citations
37	Coherence controller architectures for SMP-based CC-NUMA multiprocessors. , 1997, , .		27
38	Scalable synchronous queues. Communications of the ACM, 2009, 52, 100-111.	4.5	25
39	Sandboxing transactional memory. , 2012, , .		24
40	Shared-Memory Synchronization. Synthesis Lectures on Computer Architecture, 2013, 8, 1-221.	1.3	23
41	Scalable synchronous queues. , 2006, , .		22
42	First-class user-level threads. Operating Systems Review (ACM), 1991, 25, 110-121.	1.9	21
43	Toward a Formal Semantic Framework for Deterministic Parallel Programming. Lecture Notes in Computer Science, 2011, , 460-474.	1.3	21
44	Reducing Memory Ordering Overheads in Software Transactional Memory. , 2009, , .		20
45	Software partitioning of hardware transactions. , 2015, , .		20
46	Lazy release consistency for hardware-coherent multiprocessors. , 1995, , .		19
47	Nonblocking transactions without indirection using alert-on-update. , 2007, , .		18
48	A Key-based Adaptive Transactional Memory Executor. , 2007, , .		17
49	InterWeave: A Middleware System for Distributed Shared State. Lecture Notes in Computer Science, 2000, , 207-220.	1.3	17
50	Experience with Charlotte: simplicity and function in a distributed operating system. IEEE Transactions on Software Engineering, 1989, 15, 676-685.	5.6	16
51	Nonblocking Concurrent Data Structures with Condition Synchronization. Lecture Notes in Computer Science, 2004, , 174-187.	1.3	16
52	Hybrid NOrec. ACM SIGPLAN Notices, 2011, 46, 39-52.	0.2	16
53	Synchronization without contention. Computer Architecture News, 1991, 19, 269-278.	2.5	15
54	The Lynx distributed programming language: Motivation, design and experience. Computer Languages, Systems and Structures, 1991, 16, 209-233.	0.3	15

#	Article	IF	Citations
55	Shared memory computing on clusters with symmetric multiprocessors and system area networks. ACM Transactions on Computer Systems, 2005, 23, 301-335.	0.8	15
56	Understanding and optimizing persistent memory allocation. , 2020, , .		15
57	Alert-on-update. , 2007, , .		14
58	Large-scale parallel programming: experience with BBN butterfly parallel processor. , 1988, , .		12
59	High performance synchronization algorithms for multiprogrammed multiprocessors. , 1995, , .		12
60	Scalable queue-based spin locks with timeout. ACM SIGPLAN Notices, 2001, 36, 44-52.	0.2	12
61	Synchronization without contention. ACM SIGPLAN Notices, 1991, 26, 269-278.	0.2	11
62	Hybrid NOrec. Computer Architecture News, 2011, 39, 39-52.	2.5	11
63	Dynamic enforcement of determinism in a parallel scripting language. , 2014, , .		11
64	Simplifying Transactional Memory Support in C++. Transactions on Architecture and Code Optimization, 2019, 16, 1-24.	2.0	11
65	Fastpath Speculative Parallelization. Lecture Notes in Computer Science, 2010, , 338-352.	1.3	10
66	Generic Multiversion STM. Lecture Notes in Computer Science, 2013, , 134-148.	1.3	10
67	Implementation tradeoffs in the design of flexible transactional memory support. Journal of Parallel and Distributed Computing, 2010, 70, 1068-1084.	4.1	9
68	Transactions as the Foundation of a Memory Consistency Model. Lecture Notes in Computer Science, 2010, , 20-34.	1.3	9
69	Beyond striping: the bridge multiprocessor file system. Computer Architecture News, 1989, 17, 32-39.	2.5	8
70	Evaluation of multiprocessor memory systems using off-line optimal behavior. Journal of Parallel and Distributed Computing, 1992, 15, 382-398.	4.1	7
71	Kernel-Kernel communication in a shared-memory multiprocessor. Concurrency and Computation: Practice and Experience, 1993, 5, 171-191.	0.5	7
72	Transactions and privatization in Delaunay triangulation. , 2007, , .		7

#	Article	IF	Citations
73	Exploiting high-level coherence information to optimize distributed shared state. , 2003, , .		7
74	A Fast, General System for Buffered Persistent Data Structures. , 2021, , .		7
75	Conflict Reduction in Hardware Transactions Using Advisory Locks. , 2015, , .		6
76	Safe, Fast Sharing of memcached as a Protected Library. , 2020, , .		5
77	Large-scale parallel programming: experience with BBN butterfly parallel processor. ACM SIGPLAN Notices, 1988, 23, 161-172.	0.2	4
78	Analysis of input-dependent program behavior using active profiling. , 2007, , .		4
79	An integrated hardware-software approach to flexible transactional memory. Computer Architecture News, 2007, 35, 104-115.	2.5	4
80	Software partitioning of hardware transactions. ACM SIGPLAN Notices, 2015, 50, 76-86.	0.2	4
81	Performance Improvement via Always-Abort HTM. , 2017, , .		4
82	Generality and Speed in Nonblocking Dual Containers. ACM Transactions on Parallel Computing, 2017, 3, 1-37.	1.4	3
83	Synchronization without contention. Operating Systems Review (ACM), 1991, 25, 269-278.	1.9	2
84	Transactional memory retry mechanisms. , 2008, , .		2
85	Fast dual ring queues. , 2014, , .		2
86	Improving STM performance with transactional structs. , 2017, , .		2
87	Understanding and optimizing persistent memory allocation. , 2020, , .		2
88	Nonblocking Persistent Software Transactional Memory. , 2020, , .		2
89	Transaction Safe Nonblocking Data Structures. Lecture Notes in Computer Science, 2007, , 488-489.	1.3	2
90	An Unbounded Nonblocking Double-Ended Queue. , 2016, , .		1

#	Article	IF	Citations
91	Leveraging hardware TM in Haskell. , 2019, , .		1
92	Coherence controller architectures for SMP-based CC-NUMA multiprocessors. Computer Architecture News, 1997, 25, 219-228.	2.5	1
93	High performance synchronization algorithms for multiprogrammed multiprocessors. ACM SIGPLAN Notices, 1995, 30, 199-206.	0.2	0
94	Efficient shared memory with minimal hardware support. Computer Architecture News, 1995, 23, 29-35.	2.5	0
95	Improving STM performance with transactional structs. ACM SIGPLAN Notices, 2017, 52, 186-196.	0.2	0