Ali Afzali-Kusha

List of Publications by Citations

99 papers	1,079 citations	17 h-index	28 g-index
140 ext. papers	1,492 ext. citations	2.9 avg, IF	4.89 L-index

#	Paper	IF	Citations
99	Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 1352-1361	2.6	97
98	Substrate Noise Coupling in SoC Design: Modeling, Avoidance, and Validation. *Proceedings of the IEEE*, **2006**, 94, 2109-2138	14.3	76
97	RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 393-401	2.6	71
96	RAP-CLA: A Reconfigurable Approximate Carry Look-Ahead Adder. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 1089-1093	3.5	55
95	TOSAM: An Energy-Efficient Truncation- and Rounding-Based Scalable Approximate Multiplier. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 1161-1173	2.6	42
94	A near-threshold 7T SRAM cell with high write and read margins and low write time for sub-20 nm FinFET technologies. *The Integration VLSI Journal*, **2015**, 50, 91-106	1.4	41
93	Data Encoding Techniques for Reducing Energy Consumption in Network-on-Chip. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 675-685	2.6	32
92	Block-Based Carry Speculative Approximate Adder for Energy-Efficient Applications. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 137-141	3.5	28
91	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 2530-2541	2.6	26
90	Dynamic Voltage and Frequency Scheduling for Embedded Processors Considering Power/Performance Tradeoffs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 1931-1935	2.6	25
89	An Ultra Low-Power Memristive Neuromorphic Circuit for Internet of Things Smart Sensors. *IEEE Internet of Things Journal*, **2018**, 5, 1011-1022	10.7	22
88	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 421-433	2.6	21
87	TheSPoT: Thermal Stress-Aware Power and Temperature Management for Multiprocessor Systems-on-Chip. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 1532-1545	2.5	21
86	TruncApp: A truncation-based approximate divider for energy efficient DSP applications **2017**,		20
85	Spiral: A heuristic mapping algorithm for network on chip. *IEICE Electronics Express*, **2007**, 4, 478-484	0.5	20
84	PHAX: Physical Characteristics Aware Ex-Situ Training Framework for Inverter-Based Memristive Neuromorphic Circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 1602-1613	2.5	17
83	Statistical Design Optimization of FinFET SRAM Using Back-Gate Voltage. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 1911-1916	2.6	17

82	Res-DNN: A Residue Number System-Based DNN Accelerator Unit. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2020**, 67, 658-671	3.9	17
81	Negative Exponential Distribution Traffic Pattern for Power/Performance Analysis of Network on Chips **2009**,		16
80	An energy efficient routing protocol for cluster-based wireless sensor networks using ant colony optimization **2008**,		16
79	A Theoretical Framework for Quality Estimation and Optimization of DSP Applications Using Low-Power Approximate Adders. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 327-340	3.9	15
78	Dynamic Flip-Flop Conversion: A Time-Borrowing Method for Performance Improvement of Low-Power Digital Circuits Prone to Variations. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 2724-2727	2.6	15
77	SEERAD: A high speed yet energy-efficient rounding-based approximate divider **2016**,		14
76	Ground plane SOI MOSFET based SRAM with consideration of process variation **2010**,		13
75	Statistical model for subthreshold current considering process variations **2010**,		13
74	A heuristic machine learning-based algorithm for power and thermal management of heterogeneous MPSoCs **2015**,		12
73	Lifetime improvement by exploiting aggressive voltage scaling during runtime of error-resilient applications. *The Integration VLSI Journal*, **2018**, 61, 29-38	1.4	12
72	PX-CGRA: Polymorphic approximate coarse-grained reconfigurable architecture **2018**,		12
71	An efficent dynamic multicast routing protocol for distributing traffic in NOCs **2009**,		12
70	POLAR: A Pipelined/Overlapped FPGA-Based LSTM Accelerator. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 838-842	2.6	11
69	X-CGRA: An Energy-Efficient Approximate Coarse-Grained Reconfigurable Architecture. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 2558-2571	2.5	11
68	Toward Approximate Computing for Coarse-Grained Reconfigurable Architectures. *IEEE Micro*, **2018**, 38, 63-72	1.8	11
67	All-Region Statistical Model for Delay Variation Based on Log-Skew-Normal Distribution. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 1503-1508	2.5	10
66	Robust neuromorphic computing in the presence of process variation **2017**,		9
65	A high speed subthreshold SRAM cell design **2009**,		9

64	Subthreshold 1-Bit Full Adder Cells in sub-100 nm Technologies **2007**,		9
63	OCTAN: An On-Chip Training Algorithm for Memristive Neuromorphic Circuits. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 4687-4698	3.9	8
62	Clock Delayed Domino Logic With Efficient Variable Threshold Voltage Keeper. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2007**, 15, 125-134	2.6	8
61	Low Energy yet Reliable Data Communication Scheme for Network-on-Chip. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 1892-1904	2.5	7
60	Low power and robust 8T/10T subthreshold SRAM cells **2012**,		7
59	A low-power and low-energy flexible GF(p) elliptic-curve cryptography processor. *Journal of Zhejiang University: Science C*, **2010**, 11, 724-736		7
58	Interstice: Inverter-Based Memristive Neural Networks Discretization for Function Approximation Applications. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 1578-1588	2.6	7
57	Circuit-Level Techniques for Logic and Memory Blocks in Approximate Computing Systemsx. *Proceedings of the IEEE*, **2020**, 108, 2150-2177	14.3	7
56	An Energy-Efficient, Yet Highly-Accurate, Approximate Non-Iterative Divider **2018**,		6
55	High-performance low-leakage regions of nano-scaled CMOS digital gates under variations of threshold voltage and mobility. *Journal of Zhejiang University: Science C*, **2012**, 13, 460-471		6
54	Low Standby Power and Robust FinFET Based SRAM Design **2008**,		6
53	PAMPR: Power-aware and minimum path routing algorithm for NoCs **2008**,		6
52	A low-leakage and high-writable SRAM cell with back-gate biasing in FinFET technology. *Journal of Computational Electronics*, **2019**, 18, 519-526	1.8	5
51	A FinFET SRAM cell design with BTI robustness at high supply voltages and high yield at low supply voltages. *International Journal of Circuit Theory and Applications*, **2015**, 43, 2011-2024	2	5
50	An efficient reliability simulation flow for evaluating the hot carrier injection effect in CMOS VLSI circuits **2012**,		5
49	Forecasting-Based Dynamic Virtual Channels Allocation for Power Optimization of Network-on-Chips **2009**,		5
48	Low-latency Multi-Level Mesh Topology for NoCs **2006**,		5
47	Timing variation-aware custom instruction extension technique **2011**,		4

46	Low-Power Low-Energy Prime-Field ECC Processor Based on Montgomery Modular Inverse Algorithm **2009**,		4
45	Efficient clustering of wireless sensor networks based on memetic algorithm **2008**,		4
44	Serial Bus Encoding for Low Power Application **2006**,		4
43	Exponentially Tapering Ground Wires for Elmore Delay Reduction in On Chip Interconnects **2006**,		4
42	Novel High Speed and Low Power Single and Double Edge-Triggered Flip-Flops **2006**,		4
41	Double-edge Triggered Level Converter Flip-Flop with Feedback **2006**,		4
40	Efficient Critical Path Identification Based on Viability Analysis Method Considering Process Variations. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2668-2672	2.6	3
39	Offline Training Improvement of Inverter-Based Memristive Neural Networks Using Inverter Voltage Characteristic Smoothing. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 3442-3446	3.5	3
38	ACHILLES: Accuracy-Aware High-Level Synthesis Considering Online Quality Management. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 1452-1465	2.5	3
37	An accurate analytical IV model for sub-90-nm MOSFETs and its application to read static noise margin modeling. *Journal of Zhejiang University: Science C*, **2012**, 13, 58-70		3
36	Low power 4-bit full adder cells in subthreshold regime **2010**,		3
35	An efficient threshold voltage model for ultra thin body double gate/SOI MOSFETs **2009**,		3
34	Adaptive routing using context-aware agents for networks on chips **2009**,		3
33	Decoupling capacitor optimization for nanotechnology designs **2008**,		3
32	Low-power data encoding/decoding for energy-efficient static random access memory design. *IET Circuits, Devices and Systems*, **2019**, 13, 1152-1159	1.1	3
31	DART: A Framework for Determining Approximation Levels in an Approximable Memory Hierarchy. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 273-286	2.6	3
30	LATIM: Loading-Aware Offline Training Method for Inverter-Based Memristive Neural Networks. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 68, 3346-3350	3.5	3
29	Reliability Enhancement of Inverter-Based Memristor Crossbar Neural Networks Using Mathematical Analysis of Circuit Non-Idealities. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 68, 4310-4323	3.9	3

28	Embedded Complex Floating Point Hardware Accelerator **2014**,		2
27	A thermal stress-aware algorithm for power and temperature management of MPSoCs **2015**,		2
26	Improving efficiency of extensible processors by using approximate custom instructions **2014**,		2
25	Process variation tolerant SRAM cell design using additive model considering NBTI effect **2012**,		2
24	A RESURF LDMOSFET with a dummy gate on partial SOI. *Journal of the Korean Physical Society*, **2012**, 60, 842-848	0.6	2
23	COMRA: An efficient low-energy core mapping and routing path allocation algorithm for heterogeneous NoCs **2009**,		2
22	Static power optimization of a Full-Adder under Front-End of Line systematic variations **2009**,		2
21	An Efficient Clocking Scheme for On-Chip Communications **2006**,		2
20	Optimizing High Speed Flip-Flop Using Genetic Algorithm **2006**,		2
19	RandShift: An Energy-Efficient Fault-Tolerant Method in Secure Nonvolatile Main Memory. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 287-291	2.6	2
18	Loading-Aware Reliability Improvement of Ultra-Low Power Memristive Neural Networks. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 68, 3411-3421	3.9	2
17	O□DNN: A Hybrid DSP-LUT-Based Processing Unit With Operation Packing and Out-of-Order Execution for Efficient Realization of Convolutional Neural Networks on FPGA Devices. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2020**, 67, 3056-3069	3.9	1
16	An Efficient False Path-Aware Heuristic Critical Path Selection Method with High Coverage of the Process Variation Space. *ACM Transactions on Design Automation of Electronic Systems*, **2018**, 23, 1-25	1.5	1
15	A new merit function for custom instruction selection under an area budget constraint. *Design Automation for Embedded Systems*, **2013**, 17, 1-25	0.6	1
14	Robust polysilicon gate FinFET SRAM design using dynamic back-gate bias **2013**,		1
13	LLA: A low-latency asynchronous control with applications **2009**,		1
12	Very low-power flexible GF(p) elliptic-curve crypto-processor for non-time-critical applications **2009** ,		1
11	NBTI tolerant 4T double-gate SRAM design **2009**,		1

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10	Stall Power Reduction in Pipelined Architecture Processors **2008**,		1
9	Design centering scheme for robust SRAM cell design **2008**,		1
8	A low-power high-throughput link splitting router for NoCs. *Journal of Zhejiang University: Science A* , **2008**, 9, 1708-1714	2.1	1
7	A Mesochronous Technique for Communication in Network on Chips **2006**,		1
6	Quantitative Comparison of Optical and Electrical H, X, and Y clock Distribution Networks **2007**,		1
5	Improved Assertion Lifetime via Assertion-Based Testing Methodology **2006**,		1
4	CD-DFT: A Current-Difference Design-for-Testability to Detect Short Defects of STT-MRAM Under Process Variations. *IEEE Transactions on Device and Materials Reliability*, **2021**, 21, 436-443	1.6	1
3	An Adaptive Memory Side Encryption Method for Improving Security and Lifetime of PCM-based Main Memory. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	1
2	Dynamic power management with fuzzy decision support system. *IEICE Electronics Express*, **2008**, 5, 789-795	0.5	
1	OPTIMA: An Approach for Online Management of Cache Approximation Levels in Approximate Processing Systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 29, 434-446	2.6	