Ali Afzali-Kusha

List of Publications by Year
in descending order

139 papers	1,819 citations	361413 20 h-index	345221 36 g-index
140 all docs	140 docs citations	140 times ranked	1158 citing authors

#	Article	IF	Citations
1	Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1352-1361.	3.1	188
2	RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 393-401.	3.1	130
3	Substrate Noise Coupling in SoC Design: Modeling, Avoidance, and Validation. Proceedings of the IEEE, 2006, 94, 2109-2138.	21.3	104
4	RAP-CLA: A Reconfigurable Approximate Carry Look-Ahead Adder. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1089-1093.	3.0	98
5	TOSAM: An Energy-Efficient Truncation- and Rounding-Based Scalable Approximate Multiplier. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1161-1173.	3.1	93
6	Approximate Reverse Carry Propagate Adder for Energy-Efficient DSP Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2530-2541.	3.1	58
7	A near-threshold 7T SRAM cell with high write and read margins and low write time for sub-20 nm FinFET technologies. The Integration VLSI Journal, 2015, 50, 91-106.	2.1	56
8	Data Encoding Techniques for Reducing Energy Consumption in Network-on-Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 675-685.	3.1	44
9	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 421-433.	3.1	43
10	Block-Based Carry Speculative Approximate Adder for Energy-Efficient Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 137-141.	3.0	43
11	Res-DNN: A Residue Number System-Based DNN Accelerator Unit. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 658-671.	5.4	37
12	Dynamic Voltage and Frequency Scheduling for Embedded Processors Considering Power/Performance Tradeoffs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1931-1935.	3.1	34
13	TruncApp: A truncation-based approximate divider for energy efficient DSP applications. , 2017, , .		33
14	An Ultra Low-Power Memristive Neuromorphic Circuit for Internet of Things Smart Sensors. IEEE Internet of Things Journal, 2018, 5, 1011-1022.	8.7	32
15	POLAR: A Pipelined/Overlapped FPGA-Based LSTM Accelerator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 838-842.	3.1	32
16	X-CGRA: An Energy-Efficient Approximate Coarse-Grained Reconfigurable Architecture. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2558-2571.	2.7	31
17	A Theoretical Framework for Quality Estimation and Optimization of DSP Applications Using Low-Power Approximate Adders. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 327-340.	5.4	30
18	PX-CGRA: Polymorphic approximate coarse-grained reconfigurable architecture. , 2018, , .		29

#	Article	IF	Citations
19	SEERAD: A High Speed yet Energy-Efficient Rounding-based Approximate Divider. , 2016, , .		29
20	TheSPoT: Thermal Stress-Aware Power and Temperature Management for Multiprocessor Systems-on-Chip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1532-1545.	2.7	26
21	Spiral: A heuristic mapping algorithm for network on chip. IEICE Electronics Express, 2007, 4, 478-484.	0.8	25
22	Statistical Design Optimization of FinFET SRAM Using Back-Gate Voltage. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1911-1916.	3.1	25
23	Negative Exponential Distribution Traffic Pattern for Power/Performance Analysis of Network on Chips. , 2009, , .		24
24	A heuristic machine learning-based algorithm for power and thermal management of heterogeneous MPSoCs. , 2015, , .		21
25	An energy efficient routing protocol for cluster-based wireless sensor networks using ant colony optimization. , 2008, , .		20
26	PHAX: Physical Characteristics Aware <italic>Ex-Situ</italic> Training Framework for Inverter-Based Memristive Neuromorphic Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1602-1613.	2.7	20
27	Clock Delayed Domino Logic With Efficient Variable Threshold Voltage Keeper. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 125-134.	3.1	19
28	An efficent dynamic multicast routing protocol for distributing traffic in NOCs. , 2009, , .		18
29	Dynamic Flip-Flop Conversion: A Time-Borrowing Method for Performance Improvement of Low-Power Digital Circuits Prone to Variations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2724-2727.	3.1	18
30	All-Region Statistical Model for Delay Variation Based on Log-Skew-Normal Distribution. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1503-1508.	2.7	17
31	Toward Approximate Computing for Coarse-Grained Reconfigurable Architectures. IEEE Micro, 2018, 38, 63-72.	1.8	16
32	Circuit-Level Techniques for Logic and Memory Blocks in Approximate Computing Systemsx. Proceedings of the IEEE, 2020, 108, 2150-2177.	21.3	16
33	Statistical model for subthreshold current considering process variations. , 2010, , .		15
34	A low-leakage and high-writable SRAM cell with back-gate biasing in FinFET technology. Journal of Computational Electronics, 2019, 18, 519-526.	2.5	15
35	Ground plane SOI MOSFET based SRAM with consideration of process variation. , 2010, , .		14
36	Lifetime improvement by exploiting aggressive voltage scaling during runtime of error-resilient applications. The Integration VLSI Journal, 2018, 61, 29-38.	2.1	14

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37	Subthreshold 1-Bit Full Adder Cells in sub-100 nm Technologies. , 2007, , .		12
38	Robust neuromorphic computing in the presence of process variation. , 2017, , .		12
39	OCTAN: An On-Chip Training Algorithm for Memristive Neuromorphic Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4687-4698.	5.4	12
40	Low Standby Power and Robust FinFET Based SRAM Design. , 2008, , .		11
41	A high speed subthreshold SRAM cell design. , 2009, , .		11
42	An Energy-Efficient, Yet Highly-Accurate, Approximate Non-Iterative Divider. , 2018, , .		11
43	An efficient reliability simulation flow for evaluating the hot carrier injection effect in CMOS VLSI circuits. , 2012, , .		10
44	Forecasting-Based Dynamic Virtual Channels Allocation for Power Optimization of Network-on-Chips. , 2009, , .		9
45	Low power and robust 8T/10T subthreshold SRAM cells. , 2012, , .		9
46	Interstice: Inverter-Based Memristive Neural Networks Discretization for Function Approximation Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1578-1588.	3.1	9
47	Low-latency Multi-Level Mesh Topology for NoCs. , 2006, , .		8
48	PAMPR: Power-aware and minimum path routing algorithm for NoCs. , 2008, , .		8
49	A low-power and low-energy flexible GF(p) elliptic-curve cryptography processor. Journal of Zhejiang University: Science C, 2010, 11, 724-736.	0.7	8
50	Low Energy yet Reliable Data Communication Scheme for Network-on-Chip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1892-1904.	2.7	8
51	Reliability Enhancement of Inverter-Based Memristor Crossbar Neural Networks Using Mathematical Analysis of Circuit Non-Idealities. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4310-4323.	5.4	8
52	Novel High Speed and Low Power Single and Double Edge-Triggered Flip-Flops. , 2006, , .		7
53	Double-edge Triggered Level Converter Flip-Flop with Feedback. , 2006, , .		7
54	Adaptive routing using context-aware agents for networks on chips. , 2009, , .		7

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55	High-performance low-leakage regions of nano-scaled CMOS digital gates under variations of threshold voltage and mobility. Journal of Zhejiang University: Science C, 2012, 13, 460-471.	0.7	7
56	A FinFET SRAM cell design with BTI robustness at high supply voltages and high yield at low supply voltages. International Journal of Circuit Theory and Applications, 2015, 43, 2011-2024.	2.0	7
57	DART: A Framework for Determining Approximation Levels in an Approximable Memory Hierarchy. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 273-286.	3.1	7
58	Low-Power Low-Energy Prime-Field ECC Processor Based on Montgomery Modular Inverse Algorithm. , 2009, , .		6
59	Timing variation-aware custom instruction extension technique. , 2011, , .		6
60	Exponentially Tapering Ground Wires for Elmore Delay Reduction in On Chip Interconnects. , 2006, , .		5
61	Serial Bus Encoding for Low Power Application. , 2006, , .		5
62	A High-Speed and Low-Power Voltage Controlled Oscillator in 0.18-Î¼m CMOS Process. , 2007, , .		5
63	Efficient clustering of wireless sensor networks based on memetic algorithm. , 2008, , .		5
64	An accurate analytical Iâ€“V model for sub-90-nm MOSFETs and its application to read static noise margin modeling. Journal of Zhejiang University: Science C, 2012, 13, 58-70.	0.7	5
65	Embedded Complex Floating Point Hardware Accelerator. , 2014, , .		5
66	Lowâ€power data encoding/decoding for energyâ€efficient static random access memory design. IET Circuits, Devices and Systems, 2019, 13, 1152-1159.	1.4	5
67	LATIM: Loading-Aware Offline Training Method for Inverter-Based Memristive Neural Networks. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3346-3350.	3.0	5
68	Low Power Combinational Multipliers using Data-driven Signal Gating. , 2006, , .		4
69	Decoupling capacitor optimization for nanotechnology designs. , 2008, , .		4
70	Realistic CNFET based SRAM cell design for better write stability. , 2009, , .		4
71	Efficient Critical Path Identification Based on Viability Analysis Method Considering Process Variations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2668-2672.	3.1	4
72	RandShift: An Energy-Efficient Fault-Tolerant Method in Secure Nonvolatile Main Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 287-291.	3.1	4

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73	Offline Training Improvement of Inverter-Based Memristive Neural Networks Using Inverter Voltage Characteristic Smoothing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3442-3446.	3.0	4
74	CD-DFT: A Current-Difference Design-for-Testability to Detect Short Defects of STT-MRAM Under Process Variations. IEEE Transactions on Device and Materials Reliability, 2021, 21, 436-443.	2.0	4
75	Stall Power Reduction in Pipelined Architecture Processors. , 2008, , .		3
76	A compact current-voltage model for carbon nanotube field effect transistors. , 2008, , .		3
77	An efficient threshold voltage model for ultra thin body double gate/SOI MOSFETs. , 2009, , .		3
78	Static power optimization of a Full-Adder under Front-End of Line systematic variations. , 2009, , .		3
79	Low power 4-bit full adder cells in subthreshold regime. , 2010, , .		3
80	Modeling of Hot Carrier induced substrate current and degradation in triple gate bulk FinFETs. , 2010, , .		3
81	A RESURF LDMOSFET with a dummy gate on partial SOI. Journal of the Korean Physical Society, 2012, 60, 842-848.	0.7	3
82	Improving efficiency of extensible processors by using approximate custom instructions. , 2014, , .		3
83	A Thermal Stress-Aware Algorithm for Power and Temperature Management of MPSoCs. , 2015, , .		3
84	ACHILLES: Accuracy-Aware High-Level Synthesis Considering Online Quality Management. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1452-1465.	2.7	3
85	Loading-Aware Reliability Improvement of Ultra-Low Power Memristive Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 3411-3421.	5.4	3
86	An Adaptive Memory-Side Encryption Method for Improving Security and Lifetime of PCM-Based Main Memory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1744-1756.	2.7	3
87	SySCIM: SystemC-AMS Simulation of Memristive Computation In-Memory. , 2022, , .		3
88	Improved Assertion Lifetime via Assertion-Based Testing Methodology. , 2006, , .		2
89	A Very Fast and Low Power Pseudo-Incrementer for Address Bus Encoder/Decoder. , 2006, , .		2
90	A Mesochronous Technique for Communication in Network on Chips. , 2006, , .		2

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91	An Efficient Clocking Scheme for On-Chip Communications. , 2006, , .		2
92	Optimizing High Speed Flip-Flop Using Genetic Algorithm. , 2006, , .		2
93	Quantitative Comparison of Optical and Electrical H, X, and Y clock Distribution Networks. , 2007, , .		2
94	Power management by brain emotional learning algorithm. , 2007, , .		2
95	Novel MOS Decoupling Capacitor Optimization Technique for Nanotechnologies. , 2009, , .		2
96	COMRA: An efficient low-energy core mapping and routing path allocation algorithm for heterogeneous NoCs. , 2009, , .		2
97	RATC: A robust topology control algorithm for heterogeneous wireless sensor networks. , 2009, , .		2
98	Process variation tolerant SRAM cell design using additive model considering NBTI effect. , 2012, , .		2
99	An Efficient False Path-Aware Heuristic Critical Path Selection Method with High Coverage of the Process Variation Space. ACM Transactions on Design Automation of Electronic Systems, 2018, 23, 1-25.	2.6	2
100	Oâ€DNN: A Hybrid DSP-LUT-Based Processing Unit With Operation Packing and Out-of-Order Execution for Efficient Realization of Convolutional Neural Networks on FPGA Devices. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3056-3069.	5.4	2
101	Adaptive Neural Network Model for SOI-MOSFET I-V Characteristic Including Self-Heating Effect. , 2006, , .		1
102	Subthreshold Pass Transistor Logic for Ultra-Low Power Operation. , 2007, , .		1
103	A low-power high-throughput link splitting router for NoCs. Journal of Zhejiang University: Science A, 2008, 9, 1708-1714.	2.4	1
104	Design centering scheme for robust SRAM cell design. , 2008, , .		1
105	Low-power high-performance logic style for low-voltage CMOS technologies. , 2008, , .		1
106	Low-power flexible GF(p) elliptic-curve cryptography processor. , 2008, , .		1
107	LLA: A low-latency asynchronous control with applications. , 2009, , .		1
108	Very low-power flexible GF(p) elliptic-curve crypto-processor for non-time-critical applications. , 2009, , .		1

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109	High-temperature CNFET charactristics. , 2009, , .		1
110	NBTI tolerant 4T double-gate SRAM design. , 2009, , .		1
111	Modeling of Floating-Body effect on Negative Bias Temperature Instability degradation of double-gate MOSFETs. , 2010, , .		1
112	Analytical modeling of read stability metric of SRAM cell in nanoscale era. , 2010, , .		1
113	Low-power and robust SRAM cells based on asymmetric FinFET structures. , 2012, , .		1
114	A new merit function for custom instruction selection under an area budget constraint. Design Automation for Embedded Systems, 2013, 17, 1-25.	1.0	1
115	Robust polysilicon gate FinFET SRAM design using dynamic back-gate bias. , 2013, , .		1
116	Self-impact of NBTI effect on the degradation rate of threshold voltage in PMOS transistors. , 2013, , .		1
117	Capturing and mitigating the NBTI effect during the design flow for extensible processors. , 2013, , .		1
118	Improving efficiency of extensible processors by using approximate custom instructions. , 2014, , .		1
119	A New Fair Dynamic Routing Algorithm for Avoiding Hot Spots in NoCs. , 2006, , .		0
120	A New Oscillator with Effective Phase-Noise/Power Performance. , 2007, , .		0
121	Power management with fuzzy decision support system. , 2007, , .		0
122	A Novel Method to Reduce Phase Noise in LC VCO Using a New Tail-Switching Technique. , 2007, , .		0
123	Power efficient switches with dynamic virtual channel allocation for network-on-chips. , 2008, , .		0
124	Dynamic power management with fuzzy decision support system. IEICE Electronics Express, 2008, 5, 789-795.	0.8	0
125	A robust method to estimate Power and Delay for Digital Integrated Circuits. , 2009, , .		0
126	Analytical modeling of Hot Carrier Injection induced degradation in triple gate bulk FinFETs. , 2009, , .		0

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127	V<inf>th</inf>-control method in double gate field effect transistor domino circuits. , 2009, , .		0
128	Modeling effect of Negative Bias Temperature Instability on potential distribution and degradation of double-gate MOSFETs. , 2009, , .		0
129	A surface field based model for ultra thin body undoped symmetric DG MOSFETs. , 2009, , .		0
130	Analytical modeling of Negative Bias Temperature Instability in triple gate MOSFETs. , 2009, , .		0
131	Joint-PDF of timing and power of nano-scaled CMOS digital gates due to channel length variation. , 2010, , .		0
132	Statistical delay modeling of read operation of SRAMs due to channel length variation. , 2010, , .		0
133	A new block-based SSTA method considering within-die variation. , 2010, , .		0
134	A subthreshold SRAM cell tolerant to random dopant fluctuations. , 2010, , .		0
135	Simulation of lateral effect in emitter region of silicon solar cells for concentrated sunlight. , 2011, , .		0
136	Dynamic Flip-Flop conversion to tolerate process variation in low power circuits. , 2014, , .		0
137	Dynamic Flip-Flop conversion to tolerate process variation in low power circuits. , 2014, , .		0
138	OPTIMA: An Approach for Online Management of Cache Approximation Levels in Approximate Processing Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 434-446.	3.1	0
139	AÂ²P-MANN: Adaptive Attention Inference Hops Pruned Memory-Augmented Neural Networks. IEEE Transactions on Neural Networks and Learning Systems, 2022, PP, 1-13.	11.3	0