Sylvain Maitrejean

List of Publications by Year
in descending order

56	1,190	430874 18	434195 31
papers	citations	h-index	g-index

59	59	59	1210
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Electrical Behavior of Phase-Change Memory Cells Based on GeTe. IEEE Electron Device Letters, 2010, 31, 488-490.	3.9	124
2	Investigations of titanium nitride as metal gate material, elaborated by metal organic atomic layer deposition using TDMAT and NH3. Microelectronic Engineering, 2005, 82, 248-253.	2.4	97
3	Carbon-doped GeTe: A promising material for Phase-Change Memories. Solid-State Electronics, 2011, 65-66, 197-204.	1.4	73
4	Challenges for 3D IC integration: bonding quality and thermal management. , 2007, , .		68
5	Effect of carbon doping on the structure of amorphous GeTe phase change material. Applied Physics Letters, 2011, 99, .	3.3	60
6	Impact of Oxidation on Ge₂Sb₂Te₅and GeTe Phase-Change Properties. Journal of the Electrochemical Society, 2012, 159, H373-H377.	2.9	58
7	Undulation of sub-100nm porous dielectric structures: A mechanical analysis. Applied Physics Letters, 2007, 91, .	3.3	50
8	Enabling technologies for 3D chip stacking. , 2008, , .		38
9	A Novel Programming Technique to Boost Low-Resistance State Performance in Ge-Rich GST Phase Change Memory. IEEE Transactions on Electron Devices, 2014, 61, 1246-1254.	3.0	38
10	Evidence of Germanium precipitation in phase-change Ge1â^'xTex thin films by Raman scattering. Applied Physics Letters, 2009, 95, 031908.	3.3	37
11	Crosslinking impact of mesoporous MSQ films used in microelectronic interconnections on mechanical properties. Thin Solid Films, 2006, 495, 124-129.	1.8	35
12	Three dimensional chip stacking using a wafer-to-wafer integration. , 2007, , .		35
13	Experimental measurements of electron scattering parameters in Cu narrow lines. Microelectronic Engineering, 2006, 83, 2396-2401.	2.4	34
14	Evolution of Cu microstructure and resistivity during thermal treatment of damascene line: Influence of line width and temperature. Microelectronic Engineering, 2007, 84, 2723-2728.	2.4	34
15	Conduction regime in innovative carbon nanotube via interconnect architectures. Applied Physics Letters, 2007, 91, 252107.	3.3	30
16	Study of low temperature MOCVD deposition of TiN barrier layer for copper diffusion in high aspect ratio through silicon vias. Microelectronic Engineering, 2014, 120, 127-132.	2.4	30
17	Integration of Cu/SiOC in Cu dual damascene interconnect for 0.1-Î¼m technology. Microelectronic Engineering, 2002, 64, 35-42.	2.4	27
18	Material engineering of GexTe100â^'x compounds to improve phase-change memory performances. Solid-State Electronics, 2013, 89, 93-100.	1.4	25

#	Article	IF	Citations
19	Vibrational properties and stabilization mechanism of the amorphous phase of doped GeTe. Physical Review B, 2013, 88, .	3.2	24
20	Investigations of the interface stability in HfO2â€“metal electrodes. Microelectronic Engineering, 2003, 70, 384-391.	2.4	21
21	Crystallization study of â€œmelt quenchedâ€•amorphous GeTe by transmission electron microscopy for phase change memory applications. Applied Physics Letters, 2011, 99, 243103.	3.3	20
22	Crystallization of Ge2Sb2Te5 nanometric phase change material clusters made by gas-phase condensation. Applied Physics Letters, 2012, 101, 233113.	3.3	17
23	Dependence of CMP-induced delamination on number of low-k dielectric films stacked. Microelectronic Engineering, 2006, 83, 2072-2076.	2.4	16
24	32nm node BEOL integration with an extreme low-k porous SiOCH dielectric k=2.3. Microelectronic Engineering, 2010, 87, 316-320.	2.4	16
25	GeTe phase change material and Ti based electrode: Study of thermal stability and adhesion. Microelectronic Engineering, 2011, 88, 817-821.	2.4	16
26	Grain morphology of Cu damascene lines. Microelectronic Engineering, 2010, 87, 383-386.	2.4	14
27	Cu grain growth in interconnects trenches â€“ Experimental characterization of the overburden effect. Microelectronic Engineering, 2008, 85, 2133-2136.	2.4	12
28	Pattern size dependence of grain growth in Cu interconnects. Scripta Materialia, 2010, 63, 965-968.	5.2	11
29	Experimental study of the minimum metal gate thickness required to fix the effective work function in metal-oxide-semiconductor capacitors. Applied Physics Letters, 2008, 92, 023503.	3.3	10
30	Cu Grain Growth in Damascene Narrow Trenches. , 2009, , .		9
31	A review of the mechanical stressors efficiency applied to the ultra-thin body & buried oxide fully depleted silicon on insulator technology. Solid-State Electronics, 2016, 117, 100-116.	1.4	9
32	Innovative process flow to achieve carbon nanotube based interconnects. Physica Status Solidi (A) Applications and Materials Science, 2008, 205, 1399-1401.	1.8	8
33	Integration of single carbon nanofibers in standard via interconnects. Applied Physics Letters, 2008, 92, 223510.	3.3	8
34	Morphological instabilities in Mg-7.7 at % Al. Scripta Materialia, 1999, 41, 1235-1240.	5.2	7
35	ToF-SIMS imaging of Cl at Cu grain boundaries in interconnects for microelectronics. Applied Surface Science, 2008, 255, 1564-1568.	6.1	7
36	The effect of Ta interface on the crystallization of amorphous phase change material thin films. Applied Physics Letters, 2014, 104, .	3.3	7

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37	Copper post-electroplating anneal: evaluation of in-line vs. furnace anneal on layer properties. Microelectronic Engineering, 2003, 70, 470-477.	2.4	6
38	Bias-stress-induced evolution of the dielectric properties of porous-ULK/ copper advanced interconnects. Microelectronic Engineering, 2005, 80, 345-348.	2.4	6
39	Fatigue of damascene copper lines under cyclic electrical loading. Microelectronic Engineering, 2007, 84, 2658-2662.	2.4	6
40	Toward the integration of a single carbon nanofibre as via interconnect. Microelectronic Engineering, 2008, 85, 1971-1974.	2.4	6
41	Texture and strain in narrow copper damascene interconnect lines: An X-ray diffraction analysis. Microelectronic Engineering, 2008, 85, 2175-2178.	2.4	5
42	Analysis by simulation of amorphization current in phase change memory applied to pillar and GST confined type cells. Microelectronic Engineering, 2011, 88, 827-832.	2.4	5
43	A study of nitrogen behavior in the formation of Ta/TaN and Ti/TaN alloyed metal electrodes on SiO2 and HfO2 dielectrics. Applied Physics Letters, 2014, 104, .	3.3	5
44	Test structure for characterizing metal thickness in damascene CMP technology. , 2008, , .		4
45	Plasma Enhanced Chemical Vapor Deposition of Conformal GeTe Layer for Phase Change Memory Applications. ECS Journal of Solid State Science and Technology, 2012, 1, Q119-Q122.	1.8	4
46	An analysis of stress evolution in stacked GAA transistors. , 2016, , .		3
47	Fracture Properties of Porous MSSQ Films: Impact of Porogen Loading and Burnout. Materials Research Society Symposia Proceedings, 2006, 914, 1.	0.1	2
48	Cu Resistivity in Narrow lines: Dedicated Experiments for Model Optimization. Materials Research Society Symposia Proceedings, 2006, 914, 1.	0.1	2
49	Work Function Tuning of Ti[sub x]Si[sub y]N[sub z] Electrodes Using Partial Saturation of Chemisorbing Surface during Pulsing Chemical Vapor Deposition. Electrochemical and Solid-State Letters, 2009, 12, H272.	2.2	2
50	Solution chemistry effects on cracking and damage evolution during chemical-mechanical planarization. Journal of Materials Research, 2010, 25, 1904-1909.	2.6	2
51	Evidence of Heterogeneous Strain during Crystallization of Ge2Sb2Te5 Thin Film. Electrochemical and Solid-State Letters, 2011, 14, H285.	2.2	2
52	Measuring the diffusion of Ti and Cu in low-k materials for microelectronic devices by EELS, EFTEM and EDX. Journal of Physics: Conference Series, 2006, 26, 77-80.	0.4	1
53	Fatigue of Damascene Copper Lines under AC Loading. Materials Research Society Symposia Proceedings, 2007, 990, 1.	0.1	1
54	Converting SOI to sSOI through Amorphization and Crystallization: Material Analysis and Device Demonstration. ECS Journal of Solid State Science and Technology, 2015, 4, P376-P381.	1.8	1

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55	Confined selective lateral epitaxial growth of 16-nm thick Ge nanostructures on SOI substrates: Advantages and challenges. Applied Surface Science, 2018, 445, 77-80.	6.1	1
56	Local lateral integration of 16-nm thick Ge nanowires on silicon on insulator substrates. Applied Physics Letters, 2018, 112, 241602.	3.3	0