Paulo Cesar Santos

List of Publications by Year
in descending order

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Version: 2024-02-01

15 papers	128 citations	2258059 3 h-index	1872680 6 g-index
15 all docs	15 docs citations	15 times ranked	66 citing authors

#	Article	IF	Citations
1	Efficient Machine Learning execution with Near-Data Processing. Microprocessors and Microsystems, 2022, 90, 104435.	2.8	2
2	Sim<mml:math xmlns:mml="http://www.w3.org/1998/Math/MathML" display="inline" id="d1e1024" altimg="si24.svg"><mml:msup><mml:mrow /><mml:mrow><mml:mn>2</mml:mn></mml:mrow></mml:msup></mml:math>PIM: A complete simulation framework for Processing-in-Memory. Journal of Systems Architecture, 2022, 128, 102528.	4.3	2
3	Enabling Near-Data Accelerators Adoption by Through Investigation of Datapath Solutions. International Journal of Parallel Programming, 2021, 49, 237-252.	1.5	4
4	Providing Plug N' Play for Processing-in-Memory Accelerators. , 2021, , .		4
5	A Compiler for Automatic Selection of Suitable Processing-in-Memory Instructions. , 2019, , .		17
6	A Technologically Agnostic Framework for Cyber-Physical and IoT Processing-in-Memory-based Systems Simulation. Microprocessors and Microsystems, 2019, 69, 101-111.	2.8	10
7	Exploiting Reconfigurable Vector Processing for Energy-Efficient Computation in 3D-Stacked Memories. Lecture Notes in Computer Science, 2019, , 262-276.	1.3	2
8	Exploring IoT platform with technologically agnostic processing-in-memory framework. , 2018, , .		5
9	Design space exploration for PIM architectures in 3D-stacked memories. , 2018, , .		11
10	Operand size reconfiguration for big data processing in memory. , 2017, , .		31
11	A generic processing in memory cycle accurate simulator under hybrid memory cube architecture. , 2017, , .		12
12	NIM: An HMC-Based Machine for Neuron Computation. Lecture Notes in Computer Science, 2017, , 28-35.	1.3	14
13	HMC and DDR Performance Trade-offs. IFIP Advances in Information and Communication Technology, 2017, , 159-171.	0.7	0
14	Large Vector Extensions Inside the HMC. , 2016, , .		7
15	Opportunities and Challenges of Performing Vector Operations inside the DRAM. , 2015, , .		7