Dr Kamalaksha Baral

List of Publications by Year
in descending order

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55	877	567281	501196
papers	citations	15 h-index	28 g-index

55	55	55	541
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	2-D Analytical Modeling of the Electrical Characteristics of Dual-Material Double-Gate TFETs With a SiO₂/HfO₂ Stacked Gate-Oxide Structure. IEEE Transactions on Electron Devices, 2017, 64, 960-968.	3.0	151
2	Device and Circuit-Level Assessment of GaSb/Si Heterojunction Vertical Tunnel-FET for Low-Power Applications. IEEE Transactions on Electron Devices, 2020, 67, 1285-1292.	3.0	91
3	2-D Analytical Drain Current Model of Double-Gate Heterojunction TFETs With a SiO₂/HfO₂ Stacked Gate-Oxide Structure. IEEE Transactions on Electron Devices, 2018, 65, 331-338.	3.0	66
4	Ultraviolet Detection Properties of p-Si/n-TiO₂Heterojunction Photodiodes Grown by Electron-Beam Evaporation and Solâ€“Gel Methods: A Comparative Study. IEEE Nanotechnology Magazine, 2016, 15, 193-200.	2.0	64
5	Electrical and ammonia gas sensing properties of poly (3, 3â€´- dialkylquaterthiophene) based organic thin film transistors fabricated by floating-film transfer method. Organic Electronics, 2017, 48, 53-60.	2.6	52
6	Colloidal ZnO Quantum Dots Based Spectrum Selective Ultraviolet Photodetectors. IEEE Photonics Technology Letters, 2017, 29, 361-364.	2.5	50
7	Temperature analysis of Ge/Si heterojunction SOI-Tunnel FET. Superlattices and Microstructures, 2017, 110, 162-170.	3.1	50
8	III-V/Si staggered heterojunction based source-pocket engineered vertical TFETs for low power applications. Superlattices and Microstructures, 2020, 142, 106494.	3.1	36
9	Investigation of DC, RF and linearity performances of a back-gated (BG) heterojunction (HJ) TFET-on-selbox-substrate (STFET): Introduction to a BG-HJ-STEFT based CMOS inverter. Microelectronics Journal, 2020, 102, 104775.	2.0	25
10	Simulation Study and Comparative Analysis of Some TFET Structures with a Novel Partial-Ground-Plane (PGP) Based TFET on SELBOX Structure. Silicon, 2020, 12, 2345-2354.	3.3	24
11	Fabrication and characterization of a ZnO quantum dots-based metalâ€“semiconductorâ€“metal sensor for hydrogen gas. Nanotechnology, 2019, 30, 395501.	2.6	21
12	Impact of heterogeneous gate dielectric on DC, RF and circuit-level performance of source-pocket engineered Ge/Si heterojunction vertical TFET. Semiconductor Science and Technology, 2020, 35, 105014.	2.0	21
13	Heating Effects of Colloidal ZnO Quantum Dots (QDs) on ZnO QD/CdSe QD/MoOx Photodetectors. IEEE Nanotechnology Magazine, 2017, 16, 1073-1080.	2.0	18
14	Impact of interface trap charges on electrical performance characteristics of a source pocket engineered Ge/Si heterojunction vertical TFET with HfO2/Al2O3 laterally stacked gate oxide. Microelectronics Reliability, 2021, 119, 114073.	1.7	18
15	Fabrication and Characterization of Titanium Dioxide Based Pd/TiO₂/Si MOS Sensor for Hydrogen Gas. IEEE Sensors Journal, 2018, 18, 3952-3959.	4.7	16
16	Poly (3, 3^{â€´}-dialkylquaterthiophene) Based Flexible Nitrogen Dioxide Gas Sensor. , 2018, 2, 1-4.		15
17	Efficiency Improvement of TiO₂ Nanorods Electron Transport Layer Based Perovskite Solar Cells by Solvothermal Etching. IEEE Journal of Photovoltaics, 2019, 9, 1699-1707.	2.5	15
18	Impact of interface trap charges on device level performances of a lateral/vertical gate stacked Ge/Si TFET-on-SELBOX-substrate. Applied Physics A: Materials Science and Processing, 2020, 126, 1.	2.3	15

#	Article	IF	Citations
19	Room temperature high hydrogen gas response in Pd/TiO ₂ /Si/Al capacitive sensor. Micro and Nano Letters, 2020, 15, 632-635.	1.3	12
20	Source pocket engineered underlap stacked-oxide cylindrical gate tunnel FETs with improved performance: design and analysis. Applied Physics A: Materials Science and Processing, 2020, 126, 1.	2.3	11
21	2-D analytical modeling of drain and gate-leakage currents of cylindrical gate asymmetric halo doped dual material-junctionless accumulation mode MOSFET. AEU - International Journal of Electronics and Communications, 2020, 116, 153071.	2.9	10
22	Deep Insight into DC/RF and Linearity Parameters of a Novel Back Gated Ferroelectric TFET on SELBOX Substrate for Ultra Low Power Applications. Silicon, 2021, 13, 3853-3863.	3.3	9
23	Performance Optimization of ZnO Nanorods ETL Based Hybrid Perovskite Solar Cells With Different Seed Layers. IEEE Transactions on Electron Devices, 2022, 69, 2494-2499.	3.0	8
24	Ultrathin body nanowire hetero-dielectric stacked asymmetric halo doped junctionless accumulation mode MOSFET for enhanced electrical characteristics and negative bias stability. Superlattices and Microstructures, 2020, 138, 106364.	3.1	7
25	Device-Level Performance Comparison of Some Pocket Engineered III-V/Si Hetero-Junction Vertical Tunnel Field Effect Transistor. , 2020, , .		7
26	Analytical Drain Current Model for Source Pocket Engineered Stacked Oxide SiO2/HfO2 Cylindrical Gate TFETs. Silicon, 2021, 13, 1731-1739.	3.3	7
27	Ferroelectric Gate Heterojunction TFET on Selective Buried Oxide (SELBOX) Substrate for Distortionless and Low Power Applications. , 2020, , .		6
28	Performance Comparison of Ge/Si Hetero-Junction Vertical Tunnel FET with and Without Gate-Drain Underlapped Structure with Application to Digital Inverter. , 2020, , .		6
29	2-D Analytical Model for Electrical Characteristics of Dual Metal Heterogeneous Gate Dielectric Double-Gate TFETs with Localized Interface Charges. Silicon, 2021, 13, 2519-2527.	3.3	5
30	Study of Temperature Sensitivity on Linearity Figures of Merit of Ge/Si Hetero-Junction Gate-Drain Underlapped Vertical Tunnel FET with heterogeneous gate dielectric structure for Improving Device Reliability. , 2020, , .		4
31	Design and Performance Assessment of HfO2/SiO2 Gate Stacked Ge/Si Heterojunction TFET on SELBOX Substrate (GSHJ-STFET). Silicon, 2022, 14, 11847-11858.	3.3	4
32	Performance Evaluation of Heterojunction SOI-Tunnel FET with Temperature. , 2017, , .		3
33	Impact of Strain on Electrical Characteristic of Double-Gate TFETs with a SiO<inf>2</inf>/RfO<inf>2</inf>Stacked Gate-Oxide Structure. , 2017, , .		3
34	DC and RF Performance Optimization of Strained Si/Si1-xGex Heterojunction SOI P-TFET. , 2018, , .		3
35	Effects of source/drain elevation and side spacer dielectric on drivability performance of non-abrupt ultra shallow junction gate underlap GAA MOSFETs. Indian Journal of Physics, 2018, 92, 171-176.	1.8	2
36	Dual Material-Stacked Hetero-Dielectric-Junctionless Accumulation Mode Nanotube MOSFET for enhanced Hot Carrier and Trapped Charges Reliability. , 2019, , .		2

#	Article	IF	Citations
37	Study and Investigation of DC and RF Performance of TFET on SEL-BOX and Conventional SOI TFET with SiO2/HfO2 Stacked Gate Structure. , 2019, , .		2
38	Impact of Gate Dielectrics on Analog/RF Performance of Double Gate Tunnel Field Effect Transistor. , 2019, , .		2
39	Low-Cost Ag/PEDOT: PSS/ZnO Quantum Dot/ITO p-n junction based Photodetector. , 2020, , .		2
40	A 2-D compact DC model for engineered nanowire JAM-MOSFETs valid for all operating regimes. Semiconductor Science and Technology, 2020, 35, 085014.	2.0	2
41	Impact of ion implantation on stacked oxide cylindrical gate junctionless accumulation mode MOSFET: An electrical and circuit level analysis. Materials Science in Semiconductor Processing, 2021, 133, 105966.	4.0	2
42	Design and Simulation of Triple Material Gate InAs/Si Heterojunction TFET on SEL-BOX Substrates: Temperature Impact Analysis. , 2021, , .		2
43	Dual-Material Ferroelectric Stacked Gate SiO<inf>2</inf>/PZT SOI Tunnel FETs with Improved Performance: Design and Analysis. , 2018, , .		1
44	Performance evaluation of double gate III-V heterojunction tunnel FETs with SiO<inf>2</inf>/HfO<inf>2</inf> Gate oxide structure. , 2018, , .		1
45	Performance Investigation of a p-Channel Hetero-Junction GaN Tunnel FET. , 2019, , .		1
46	New Topologies of a Lossless Grounded Negative Inductor Using Single CDBA. , 2019, , .		1
47	Subthreshold Swing Modeling of Gaussian Doped Double-Gate MOSFETs and its Validation Based on TCAD Simulation. , 2020, , .		1
48	Influence of Temperature on Analog/Radio Frequency Appearances of Heterojunction Cylindrical Gate Tunnel FETs. , 2020, , .		1
49	Device and Circuit-Level Performance Comparison of Vertically Grown All-Si and Ge/Si Hetero-Junction TFET. , 2020, , .		1
50	Lateral and Vertical Gate Oxide Stacking Impact on Noise Margins and Delays for the 8T SRAM Designed With Source Pocket Engineered GaSb/Si Heterojunction Vertical TFET: A Reliability Study. IEEE Transactions on Device and Materials Reliability, 2021, 21, 372-378.	2.0	1
51	A Simulation Based Study for Electrical Characteristics of SOI TFETs With Ferroelectric Stacked Gate Oxide Structure. , 2017, , .		0
52	Influence of Localized Interface Charges on Drain Current of Dual-Material Double-Gate Tunnel FETs. , 2018, , .		0
53	Performance Analysis of Nanotube Junctionless Accumulation Mode MOSFETs with Ion Implanted Doping Profile. , 2018, , .		0
54	TCAD Assessment Based Device to Circuit-Level Performance Comparison Study of Source Pocket Engineered All-Si Vertical Tunnel FET and GaSb/Si Heterojunction Vertical Tunnel FET. , 2020, , .		0

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55	A unified 2-D model for nanowire junctionless accumulation and inversion mode MOSFET in quasi-ballistic regime. Solid-State Electronics, 2022, 193, 108282.	1.4	0