

# Seongjae Cho

## List of Publications by Year in descending order

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144  
papers

1,590  
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331259

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377514

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all docs

144  
docs citations

144  
times ranked

1159  
citing authors

#	ARTICLE	IF	CITATIONS
1	RF Performance and Small-Signal Parameter Extraction of Junctionless Silicon Nanowire MOSFETs. IEEE Transactions on Electron Devices, 2011, 58, 1388-1396.	1.6	170
2	Analyses on Small-Signal Parameters and Radio-Frequency Modeling of Gate-All-Around Tunneling Field-Effect Transistors. IEEE Transactions on Electron Devices, 2011, 58, 4164-4171.	1.6	82
3	Resistive switching characteristics of Si <sub>3</sub> N <sub>4</sub> -based resistive-switching random-access memory cell with tunnel barrier for high density integration and low-power applications. Applied Physics Letters, 2015, 106, .	1.5	77
4	Scaling Effect on Silicon Nitride Memristor with Highly Doped Si Substrate. Small, 2018, 14, e1704062.	5.2	74
5	Ultrasensitive MoS <sub>2</sub> photodetector by serial nano-bridge multi-heterojunction. Nature Communications, 2019, 10, 4701.	5.8	66
6	Zinc Tin Oxide Synaptic Device for Neuromorphic Engineering. IEEE Access, 2020, 8, 130678-130686.	2.6	41
7	Simulation study on effect of drain underlap in gate-all-around tunneling field-effect transistors. Current Applied Physics, 2013, 13, 1143-1149.	1.1	40
8	Silicon-compatible compound semiconductor tunneling field-effect transistor for high performance and low standby power operation. Applied Physics Letters, 2011, 99, .	1.5	36
9	Recent Advances in Electrical Doping of 2D Semiconductor Materials: Methods, Analyses, and Applications. Nanomaterials, 2021, 11, 832.	1.9	36
10	Characterization and Optimization of Inverted-T FinFET Under Nanoscale Dimensions. IEEE Transactions on Electron Devices, 2018, 65, 3521-3527.	1.6	34
11	Fully Si compatible SiN resistive switching memory with large self-rectification ratio. AIP Advances, 2016, 6, .	0.6	33
12	Integrate-and-fire neuron circuit using positive feedback field effect transistor for low power operation. Journal of Applied Physics, 2018, 124, .	1.1	33
13	Effects of conducting defects on resistive switching characteristics of SiN <sub>x</sub> -based resistive random-access memory with MIS structure. Journal of Vacuum Science and Technology B: Nanotechnology and Microelectronics, 2015, 33, .	0.6	28
14	Nano-cone resistive memory for ultralow power operation. Nanotechnology, 2017, 28, 125207.	1.3	27
15	Fabrication and Characterization of a Thin-Body Poly-Si 1T DRAM With Charge-Trap Effect. IEEE Electron Device Letters, 2019, 40, 566-569.	2.2	27
16	Gradual bipolar resistive switching in Ni/Si <sub>3</sub> N <sub>4</sub> /n <sup>+</sup> -Si resistive-switching memory device for high-density integration and low-power applications. Solid-State Electronics, 2015, 114, 94-97.	0.8	26
17	Design and analysis of Si-based arch-shaped gate-all-around (GAA) tunneling field-effect transistor (TFET). Current Applied Physics, 2015, 15, 208-212.	1.1	24
18	Design of Poly-Si Junctionless Fin-Channel FET With Quantum-Mechanical Drift-Diffusion Models for Sub-10-nm Technology Nodes. IEEE Transactions on Electron Devices, 2016, 63, 4610-4616.	1.6	23

#	ARTICLE	IF	CITATIONS
19	Gradual switching and self-rectifying characteristics of Cu <sup>±</sup> /IGZO/p <sup>+</sup> -Si RRAM for synaptic device application. <i>Solid-State Electronics</i> , 2018, 150, 60-65.	0.8	23
20	Emulation of synaptic functions with low voltage organic memtransistor for hardware oriented neuromorphic computing. <i>Scientific Reports</i> , 2022, 12, 3808.	1.6	23
21	Design optimization of tunneling field-effect transistor based on silicon nanowire PNPN structure and its radio frequency characteristics. <i>Current Applied Physics</i> , 2012, 12, 673-677.	1.1	22
22	Double-Gate Junctionless 1T DRAM With Physical Barriers for Retention Improvement. <i>IEEE Transactions on Electron Devices</i> , 2020, 67, 1471-1479.	1.6	22
23	Uniformity Improvement of SiN <sub>x</sub> -Based Resistive Switching Memory by Suppressed Internal Overshoot Current. <i>IEEE Nanotechnology Magazine</i> , 2018, 17, 824-828.	1.1	20
24	A polycrystalline-silicon dual-gate MOSFET-based 1T-DRAM using grain boundary-induced variable resistance. <i>Applied Physics Letters</i> , 2019, 114, .	1.5	20
25	Ultrathin SiGe Shell Channel p-Type FinFET on Bulk Si for Sub-10-nm Technology Nodes. <i>IEEE Transactions on Electron Devices</i> , 2018, 65, 1290-1297.	1.6	19
26	Fabrication and Characterization of TiO <sub>x</sub> Memristor for Synaptic Device Application. <i>IEEE Nanotechnology Magazine</i> , 2020, 19, 475-480.	1.1	19
27	Resistive Switching Characteristics of Silicon Nitride-Based RRAM Depending on Top Electrode Metals. <i>IEICE Transactions on Electronics</i> , 2015, E98.C, 429-433.	0.3	17
28	Pd/IGZO/p <sup>+</sup> -Si Synaptic Device with Self-Graded Oxygen Concentrations for Highly Linear Weight Adjustability and Improved Energy Efficiency. <i>ACS Applied Electronic Materials</i> , 2020, 2, 2390-2397.	2.0	17
29	Performance Improvement of 1T DRAM by Raised Source and Drain Engineering. <i>IEEE Transactions on Electron Devices</i> , 2021, 68, 1577-1584.	1.6	16
30	Design and Analysis of Sub-10 nm Junctionless Fin-Shaped Field-Effect Transistors. <i>Journal of Semiconductor Technology and Science</i> , 2014, 14, 508-517.	0.1	16
31	Core-Shell Dual-Gate Nanowire Charge-Trap Memory for Synaptic Operations for Neuromorphic Applications. <i>Nanomaterials</i> , 2021, 11, 1773.	1.9	15
32	Simulation Study on Silicon-Based Floating Body Synaptic Transistor with Short- and Long-Term Memory Functions and Its Spike Timing-Dependent Plasticity. <i>Journal of Semiconductor Technology and Science</i> , 2016, 16, 657-663.	0.1	15
33	A Band-Engineered One-Transistor DRAM With Improved Data Retention and Power Efficiency. <i>IEEE Electron Device Letters</i> , 2019, 40, 562-565.	2.2	14
34	Room-temperature electroluminescence from germanium in an Al <sub>0.3</sub> Ga <sub>0.7</sub> As/Ge heterojunction light-emitting diode by $\Gamma^c$ -valley transport. <i>Optics Express</i> , 2012, 20, 14921.	1.7	13
35	Bipolar resistive switching with unidirectional selector function in nitride/oxide heterostructures. <i>Journal Physics D: Applied Physics</i> , 2020, 53, 435102.	1.3	13
36	A More Hardware-Oriented Spiking Neural Network Based on Leading Memory Technology and Its Application With Reinforcement Learning. <i>IEEE Transactions on Electron Devices</i> , 2021, 68, 4411-4417.	1.6	13

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37	Design and optimization of two-bit double-gate nonvolatile memory cell for highly reliable operation. IEEE Nanotechnology Magazine, 2006, 5, 180-185.	1.1	12
38	Fabrication and Analysis of Epitaxially Grown Ge <sub>1-x</sub> Sn <sub>x</sub> Microdisk Resonator With 20-nm Free-Spectral Range. IEEE Photonics Technology Letters, 2011, 23, 1535-1537.	1.3	12
39	More Accurate and Reliable Extraction of Tunneling Resistance in Tunneling FET and Verification in Small-Signal Circuit Operation. IEEE Transactions on Electron Devices, 2013, 60, 3318-3324.	1.6	12
40	Design and Characterization of Semi-Floating-Gate Synaptic Transistor. Micromachines, 2019, 10, 32.	1.4	12
41	Pulse area dependent gradual resistance switching characteristics of CMOS compatible SiN <sub>x</sub> -based resistive memory. Solid-State Electronics, 2017, 132, 109-114.	0.8	11
42	Synaptic behaviors of HfO <sub>2</sub> ReRAM by pulse frequency modulation. Solid-State Electronics, 2019, 154, 31-35.	0.8	11
43	Core-Shell Dual-Gate Nanowire Memory as a Synaptic Device for Neuromorphic Application. IEEE Journal of the Electron Devices Society, 2021, 9, 1282-1289.	1.2	11
44	Simulation of Gate-All-Around Tunnel Field-Effect Transistor with an n-Doped Layer. IEICE Transactions on Electronics, 2010, E93-C, 540-545.	0.3	11
45	Optimization of the structural complexity of artificial neural network for hardware-driven neuromorphic computing application. Applied Intelligence, 2023, 53, 6288-6306.	3.3	11
46	A Vertical 4-Bit SONOS Flash Memory and a Unique 3-D Vertical nor Array Structure. IEEE Nanotechnology Magazine, 2010, 9, 70-77.	1.1	10
47	Design and Electrical Characterization of 2-T Thyristor RAM With Low Power Consumption. IEEE Electron Device Letters, 2018, 39, 355-358.	2.2	10
48	Investigation of the Thermal Recovery From Reset Breakdown of a SiN <sub>x</sub> -Based RRAM. IEEE Transactions on Electron Devices, 2020, 67, 1600-1605.	1.6	10
49	Analysis of the Sensing Margin of Silicon and Poly-Si 1T-DRAM. Micromachines, 2020, 11, 228.	1.4	10
50	Threshold-Variation-Tolerant Coupling-Gate $\hat{\pm}$ -IGZO Synaptic Transistor for More Reliably Controllable Hardware Neuromorphic System. IEEE Access, 2021, 9, 59345-59352.	2.6	10
51	Medium-Temperature-Oxidized GeO <sub>x</sub> Resistive-Switching Random-Access Memory and Its Applicability in Processing-in-Memory Computing. Nanoscale Research Letters, 2022, 17, .	3.1	10
52	InGaAs/InP heterojunction-channel tunneling field-effect transistor for ultra-low operating and standby power application below supply voltage of 0.5ÅV. Current Applied Physics, 2013, 13, 2051-2054.	1.1	9
53	Mixed-Mode Simulation of Nanowire Ge/GaAs Heterojunction Tunneling Field-Effect Transistor for Circuit Applications. IEEE Journal of the Electron Devices Society, 2013, 1, 48-53.	1.2	9
54	A Novel One-Transistor Dynamic Random-Access Memory (1T DRAM) Featuring Partially Inserted Wide-Bandgap Double Barriers for High-Temperature Applications. Micromachines, 2018, 9, 581.	1.4	9

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55	A Quantum-Well Charge-Trap Synaptic Transistor With Highly Linear Weight Tunability. IEEE Journal of the Electron Devices Society, 2020, 8, 834-840.	1.2	9
56	Nanoscale wedge resistive-switching synaptic device and experimental verification of vector-matrix multiplication for hardware neuromorphic application. Japanese Journal of Applied Physics, 2021, 60, 050905.	0.8	9
57	Silicon-compatible bulk-type compound junctionless field-effect transistor. , 2011, , .		8
58	DIBL-Induced Program Disturb Characteristics in 32-nm NAND Flash Memory Array. IEEE Transactions on Electron Devices, 2011, 58, 3626-3629.	1.6	8
59	Design and analysis of nanowire p-type MOSFET coaxially having silicon core and germanium peripheral channel. Japanese Journal of Applied Physics, 2016, 55, 114001.	0.8	8
60	Silicon-compatible high-hole-mobility transistor with an undoped germanium channel for low-power application. Applied Physics Letters, 2013, 103, 222102.	1.5	7
61	Insertion of Ag Layer in TiN/SiN <sub>x</sub> /TiN RRAM and Its Effect on Filament Formation Modeled by Monte Carlo Simulation. IEEE Access, 2020, 8, 228720-228730.	2.6	7
62	Key factors affecting contact resistance in coplanar organic thin-film transistors. Journal Physics D: Applied Physics, 2022, 55, 405101.	1.3	7
63	Analysis of operation characteristics of junctionless poly-Si 1T-DRAM in accumulation mode. Semiconductor Science and Technology, 2019, 34, 105007.	1.0	6
64	Processing and Characterization of Ultra-thin Poly-crystalline Silicon for Memory and Logic Applications. Journal of Semiconductor Technology and Science, 2018, 18, 172-179.	0.1	6
65	Investigation of Modified 1T DRAM with Twin Gate Tunneling Field Effect Transistor for Improved Retention Characteristics. Journal of Semiconductor Technology and Science, 2020, 20, 145-150.	0.1	6
66	Improved resistive switching properties in SiO <sub>x</sub> -based resistive random-access memory cell with Ti buffer layer. Journal of Vacuum Science and Technology B: Nanotechnology and Microelectronics, 2016, 34, .	0.6	5
67	A highly reliable physics-based SPICE compact model of IGZO memristor considering the dependence on electrode metals and deposition sequence. Solid-State Electronics, 2020, 166, 107764.	0.8	5
68	Multilevel Switching Characteristics of Si <sub>3</sub> N <sub>4</sub> -Based Nano-Wedge Resistive Switching Memory and Array Simulation for In-Memory Computing Application. Electronics (Switzerland), 2020, 9, 1228.	1.8	5
69	Density functional theory study on the modification of silicon nitride surface by fluorine-containing molecules. Applied Surface Science, 2021, 554, 149481.	3.1	5
70	Improvement of Resistive Switching Characteristics of Titanium Oxide Based Nanowedge RRAM Through Nickel Silicidation. IEEE Transactions on Electron Devices, 2021, 68, 438-442.	1.6	5
71	Sub-10 nm Ge/GaAs Heterojunction-Based Tunneling Field-Effect Transistor with Vertical Tunneling Operation for Ultra-Low-Power Applications. Journal of Semiconductor Technology and Science, 2016, 16, 172-178.	0.1	5
72	Investigation and Optimization of Double-gate MPI 1T DRAM with Gate-induced Drain Leakage Operation. Journal of Semiconductor Technology and Science, 2019, 19, 165-171.	0.1	5

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73	Depletion-enhanced body-isolation (DEBI) array on SOI for highly scalable and reliable NAND flash memories. IEEE Nanotechnology Magazine, 2006, 5, 201-204.	1.1	4
74	Stacked Gated Twin-Bit (SGTB) SONOS Memory Device for High-Density Flash Memory. IEEE Nanotechnology Magazine, 2012, 11, 307-313.	1.1	4
75	Dual gate positive feedback field-effect transistor for low power analog circuit. , 2017, , .		4
76	Design Optimization and Analysis of InGaAs/InAs/InGaAs Heterojunction-Based Electron Hole Bilayer Tunneling FETs. Journal of Nanoscience and Nanotechnology, 2019, 19, 6070-6076.	0.9	4
77	Ni/GeOx/p+ Si resistive-switching random-access memory with full Si processing compatibility and its characterization and modeling. Vacuum, 2019, 161, 63-70.	1.6	4
78	Novel Au nanorod/Cu <sub>2</sub> O composite nanoparticles for a high-performance supercapacitor. RSC Advances, 2022, 12, 9112-9120.	1.7	4
79	A 2-Bit Recessed Channel Nonvolatile Memory Device With a Lifted Charge-Trapping Node. IEEE Nanotechnology Magazine, 2009, 8, 111-115.	1.1	3
80	Channel doping concentration and fin width effects on self-boosting in NAND-type SONOS flash memory array based on bulk-FinFETs. , 2009, , .		3
81	Investigation of source-to-drain capacitance by DIBL effect of silicon nanowire MOSFETs. IEICE Electronics Express, 2010, 7, 1499-1503.	0.3	3
82	Heteromaterial Gate Tunneling Field-Effect Transistor for High-Speed and Radio-Frequency Applications. Journal of Nanoscience and Nanotechnology, 2014, 14, 8136-8140.	0.9	3
83	High-performance Ge/GaAs heterojunction tunneling FET with a channel engineering for sub-0.5 V operation. Semiconductor Science and Technology, 2015, 30, 035020.	1.0	3
84	Bias Polarity Dependent Resistive Switching Behaviors in Silicon Nitride-Based Memory Cell. IEICE Transactions on Electronics, 2016, E99.C, 547-550.	0.3	3
85	Circuit-level simulation of resistive-switching random-access memory cross-point array based on a highly reliable compact model. Journal of Computational Electronics, 2018, 17, 273-278.	1.3	3
86	Compact modeling of silicon nanowire MOSFET for radio frequency applications. Microwave and Optical Technology Letters, 2011, 53, 471-473.	0.9	2
87	Simulation study on scaling limit of silicon tunneling field-effect transistor under tunneling-predominance. IEICE Electronics Express, 2012, 9, 828-833.	0.3	2
88	Design of a recessed-gate GaN-based MOSFET using a dual gate dielectric for high-power applications. Journal of the Korean Physical Society, 2014, 65, 1579-1584.	0.3	2
89	Switching and conduction mechanism of Cu/Si <sub>3</sub> N <sub>4</sub> /Si RRAM with CMOS compatibility. , 2014, , .		2
90	Analysis of Radio Frequency Performance on GaAs/InGaAs Heterojunction Tunneling Field-Effect Transistor which Applicable for Green Energy System Applications. , 2014, , .		2

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91	Analyses on RF Performances of Silicon-Compatible InGaAs-Based Planar-Type and Fin-Type Junctionless Field-Effect Transistors. <i>Journal of Nanoscience and Nanotechnology</i> , 2015, 15, 7615-7619.	0.9	2
92	An accurate simulation study on capacitance-voltage characteristics of metal-oxide-semiconductor field-effect transistors in novel structures. <i>Physica B: Condensed Matter</i> , 2017, 521, 305-311.	1.3	2
93	A Highly Scalable and Energy-Efficient 1T DRAM Embedding a SiGe Quantum Well Structure for Significant Retention Enhancement. , 2018, , .		2
94	Design and analysis of logic inverter using antimonide-based compound semiconductor junctionless transistor. <i>Applied Physics A: Materials Science and Processing</i> , 2019, 125, 1.	1.1	2
95	Microwave analysis of SiGe heterojunction double-gate tunneling field-effect transistor through its small-signal equivalent circuit. <i>International Journal of RF and Microwave Computer-Aided Engineering</i> , 2019, 29, e21678.	0.8	2
96	More physical understanding of current characteristics of tunneling field-effect transistor leveraged by gate positions and properties through dual-gate and gate-all-around structuring. <i>Applied Physics A: Materials Science and Processing</i> , 2020, 126, 1.	1.1	2
97	HfO <sub>x</sub> -based nano-wedge structured resistive switching memory device operating at sub-1/4 A current for neuromorphic computing application. <i>Semiconductor Science and Technology</i> , 2020, 35, 055002.	1.0	2
98	Process Steps for High Quality Si-Based Epitaxial Growth at Low Temperature via RPCVD. <i>Materials</i> , 2021, 14, 3733.	1.3	2
99	Reliability improvement of 1T DRAM based on feedback transistor by using local partial insulators. <i>Japanese Journal of Applied Physics</i> , 2021, 60, 104002.	0.8	2
100	Si CMOS Extension and Ge Technology Perspectives Forecast Through Metal-oxide-semiconductor Junctionless Field-effect Transistor. <i>Journal of Semiconductor Technology and Science</i> , 2016, 16, 847-853.	0.1	2
101	Optimization of Feedback FET with Asymmetric Source Drain Doping Profile. <i>Micromachines</i> , 2022, 13, 508.	1.4	2
102	Vertical AND (V-AND) array: High density, high speed, and reliable flash array. , 2007, , .		1
103	Fabrication and Characterization of GaN-based Light-emitting Diode (LED) with Triangle-type Structure. <i>Molecular Crystals and Liquid Crystals</i> , 2014, 599, 163-169.	0.4	1
104	Dependence of device performances on fin dimensions in AlGaIn/GaN recessed-gate nanoscale FinFET. , 2014, , .		1
105	A study on room-temperature photoluminescence and crystallinity of RF-sputtered GaN for a cost-effective III-V-on-Si platform. <i>Journal of the Korean Physical Society</i> , 2015, 67, 1838-1843.	0.3	1
106	Electrical Performances of InN/GaN Tunneling Field-Effect Transistor. <i>Journal of Nanoscience and Nanotechnology</i> , 2017, 17, 8355-8359.	0.9	1
107	Analysis of tunneling field-effect transistor with germanium source junction using small-signal equivalent circuit. <i>Microwave and Optical Technology Letters</i> , 2018, 60, 2922-2927.	0.9	1
108	Si-core/SiGe-shell channel nanowire FET for sub-10-nm logic technology in the THz regime. <i>ETRI Journal</i> , 2019, 41, 829-837.	1.2	1



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109	A Novel 1T DRAM with Shell/Core Dual-Gate Architecture. , 2020, , .		1
110	Recessed Channel Dual Gate Single Electron Transistors (RCDG-SETs) for Room Temperature Operation. IEICE Transactions on Electronics, 2009, E92-C, 647-652.	0.3	1
111	3-Dimensional Terraced NAND (3D TNAND) Flash Memory-Stacked Version of Folded NAND Array. IEICE Transactions on Electronics, 2009, E92-C, 653-658.	0.3	1
112	A More Accurate Analytical DC Compact Modeling of Tunneling Field-Effect Transistor for SPICE Simulation. Journal of Semiconductor Technology and Science, 2019, 19, 551-560.	0.1	1
113	Simulation of Retention Characteristics in Double-Gate Structure Multi-Bit SONOS Flash Memory. IEICE Transactions on Electronics, 2009, E92-C, 659-663.	0.3	1
114	Analytically and empirically consistent characterization of the resistive switching mechanism in a Ag conducting-bridge random-access memory device through a pseudo-liquid interpretation approach. Physical Chemistry Chemical Physics, 2021, 23, 27234-27243.	1.3	1
115	Low-pressure, low-temperature hydrogen annealing for nanoscale silicon fin rounding. , 2006, , .		0
116	Simulation study on negative read biasing effects for the reliable operation of NOR type floating gate flash memory devices. , 2007, , .		0
117	Fin flash memory cells with separated double gates. , 2007, , .		0
118	Gated Twin-Bit (GTB) nonvolatile memory device and its operation. , 2008, , .		0
119	Vertical channel double split-gate (VCDSG) flash memory. , 2008, , .		0
120	Program efficiency relying on channel conditions at NOR-type flash memory device based on silicon-on-insulator (SOI). , 2008, , .		0
121	Enhancement of erase speed using silicide drain in nanowire SONOS NAND flash memory. , 2009, , .		0
122	Design of SOI FinFET on 32 nm technology node for low standby power (LSTP) operation considering gate-induced drain leakage (GIDL). , 2009, , .		0
123	Dependence of program and erase speed on bias conditions for fully depleted channel of vertical NAND flash memory devices. , 2009, , .		0
124	Highly scalable vertical bandgap-engineered NAND flash memory. , 2010, , .		0
125	A New 1T DRAM Cell: Cone Type 1T DRAM Cell. IEICE Transactions on Electronics, 2011, E94-C, 681-685.	0.3	0
126	Simulation study on process conditions for high-speed silicon photodetector and quantum-well structuring for increased number of wavelength discriminations. , 2012, , .		0



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127	O <sub>2</sub> -Enhanced surface treatment of Ge epitaxially grown on Si for heterogeneous Ge technology. , 2014, , .		0
128	Optimization and modeling of npn-type selector for resistive RRAM in cross-point array structure. , 2014, , .		0
129	Analyses on ZnO/CdS heterojunction for design of CIGS photovoltaic device with higher accuracy. , 2014, , .		0
130	Vertical stack array of one-time programmable nonvolatile memory based on pn-junction diode and its operation scheme for faster access. IEICE Electronics Express, 2014, 11, 20131041-20131041.	0.3	0
131	Ge-on-Si photodetector with novel metallization schemes for on-chip optical interconnect. , 2015, , .		0
132	Effects of nitride trap layer properties on location of charge centroid in charge-trap flash memory. , 2017, , .		0
133	Uniformity improvement of SiN <sub>j</sub> c-based resistive switching memory by suppressed internal overshoot current. , 2017, , .		0
134	SiGe Heterojunction FinFET Towards Tera-Hertz Applications. Journal of the Korean Physical Society, 2018, 72, 527-532.	0.3	0
135	Simulation of One-Transistor Dynamic Random-Access Memory Based on Symmetric Double-Gate Si Junctionless Transistor. Journal of Nanoscience and Nanotechnology, 2018, 18, 6593-6597.	0.9	0
136	Analysis of SiGe Heterojunction Tunneling Field-Effect Transistor in the Microwave Regime Through Its Small-Signal Equivalent Circuit. , 2018, , .		0
137	Fabrication and Characterization of a Fully Si Compatible Forming-Free GeO <sub>x</sub> Resistive Switching Random-Access Memory. , 2018, , .		0
138	Improved Gradual Reset Phenomenon in SiN <sub>x</sub> -based RRAM by Diode-Connected Structure. , 2019, , .		0
139	Comparison of switching characteristics of HfO <sub>x</sub> RRAM device with different switching layer thicknesses. , 2019, , .		0
140	Design and Analysis of Core-Gate Shell-Chanel 1T DRAM. , 2020, , .		0
141	Simulation Study on Dependence of Channel Potential Self-Boosting on Device Scale and Doping Concentration in 2-D and 3-D NAND-Type Flash Memory Devices. IEICE Transactions on Electronics, 2010, E93-C, 596-601.	0.3	0
142	Design and Analysis for 3D Vertical Resistive Random Access Memory Structures with Silicon Bottom Electrodes. Journal of Nanoscience and Nanotechnology, 2017, 17, 7160-7163.	0.9	0
143	Charge Based Current-Voltage Model for the Silicon on Insulator Junctionless Field-Effect Transistor. Journal of Nanoscience and Nanotechnology, 2020, 20, 4920-4925.	0.9	0
144	Dependency of electrical performances and reliability of 28 nm logic transistor on gate oxide interface treatment methods. Applied Physics Express, 2020, 13, 101003.	1.1	0