Avaneesh K Dubey

List of Publications by Year
in descending order

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11 papers	103 citations	1937685 4 h-index	1872680 6 g-index

11 all docs	11 docs citations	11 times ranked	32 citing authors

#	Article	IF	Citations
1	Optimization for offset and kickback-noise in novel CMOS double-tail dynamic comparator: A low-power, high-speed design approach using bulk-driven load. Microelectronics Journal, 2018, 78, 1-10.	2.0	36
2	Low-power high-speed CMOS double tail dynamic comparator using self-biased amplification stage and novel latch stage. Analog Integrated Circuits and Signal Processing, 2019, 101, 307-317.	1.4	18
3	Enhanced Gain Low-Power CMOS Amplifiers: A Novel Design Approach Using Bulk-Driven Load and Introduction to GACOBA Technique. Journal of Circuits, Systems and Computers, 2018, 27, 1850204.	1.5	15
4	Design of low-power high-speed double-tail dynamic CMOS comparator using novel latch structure. , 2017, , .		9
5	Design and Analysis of an Energy-Efficient High-Speed CMOS Double-Tail Dynamic Comparator with Reduced Kickback Noise Effect. Journal of Circuits, Systems and Computers, 2019, 28, 1950157.	1.5	7
6	Design of Power Efficient Low-Offset Dynamic Latch Comparator using 90nm CMOS Process. , 2018, , .		6
7	Impact of Channel Doping Fluctuation and Metal Gate Work Function Variation in FD-SOI MOSFET for 5nm BOX Thickness. , 2019, , .		4
8	Design and Performance of High-speed Low-Offset CMOS Double-Tail Dynamic Comparators using Offset Control scheme. , 2019, , .		3
9	Enhanced slew rate, constant-g_m rail-to-rail OpAmp using 1:2 current mirror biasing technique. , 2016, , .		2
10	Design and Performance of High-Speed Energy-Efficient CMOS Double Tail Dynamic Latch Comparator Using GACOBA Load Suitable for Low Voltage Applications. Journal of Circuits, Systems and Computers, 2021, 30, 2150191.	1.5	2
11	Design and Performance of High-Speed CMOS Double-Tail Dynamic Comparator Suitable for Mixed-Signal ICs. Lecture Notes in Electrical Engineering, 2021, , 75-87.	0.4	1