Sung Woo Chung

List of Publications by Year
in descending order

58	800	623188 14	552369 26
papers	citations	h-index	g-index

58	58	58	630
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Recent thermal management techniques for microprocessors. ACM Computing Surveys, 2012, 44, 1-42.	16.1	167
2	Predictive Temperature-Aware DVFS. IEEE Transactions on Computers, 2010, 59, 127-133.	2.4	78
3	Energy-Optimal Dynamic Thermal Management: Computation and Cooling Power Co-Optimization. IEEE Transactions on Industrial Informatics, 2010, 6, 340-351.	7.2	51
4	Stabilizing CPU Frequency and Voltage for Temperature-Aware DVFS in Mobile Devices. IEEE Transactions on Computers, 2015, 64, 286-292.	2.4	48
5	Enhancing online power estimation accuracy for smartphones. IEEE Transactions on Consumer Electronics, 2012, 58, 333-339.	3.0	28
6	A Survey on Recent OS-Level Energy Management Techniques for Mobile Processing Units. IEEE Transactions on Parallel and Distributed Systems, 2018, 29, 2388-2401.	4.0	26
7	Measuring Variance between Smartphone Energy Consumption and Battery Life. Computer, 2014, 47, 59-65.	1.2	23
8	Enhancing Energy Efficiency of Multimedia Applications in Heterogeneous Mobile Multi-Core Processors. IEEE Transactions on Computers, 2017, 66, 1878-1889.	2.4	22
9	The impact of liquid cooling on 3D multi-core processors. , 2009, , .		19
10	Load Unbalancing Strategy for Multicore Embedded Processors. IEEE Transactions on Computers, 2010, 59, 1434-1440.	2.4	19
11	A Novel GPU Power Model for Accurate Smartphone Power Breakdown. ETRI Journal, 2015, 37, 157-164.	1.2	19
12	On the Thermal Attack in Instruction Caches. IEEE Transactions on Dependable and Secure Computing, 2010, 7, 217-223.	3.7	18
13	Exploiting Refresh Effect of DRAM Read Operations: A Practical Approach to Low-Power Refresh. IEEE Transactions on Computers, 2016, 65, 1507-1517.	2.4	17
14	An Adaptive Thermal Management Framework for Heterogeneous Multi-Core Processors. IEEE Transactions on Computers, 2020, 69, 894-906.	2.4	17
15	Using On-Chip Event Counters For High-Resolution, Real-Time Temperature Measurement. , 0, , .		16
16	Low-Cost Application-Aware DVFS for Multi-core Architecture. , 2008, , .		15
17	Architecting large-scale SRAM arrays with monolithic 3D integration. , 2017, , .		15
18	Exploiting Application/System-Dependent Ambient Temperature for Accurate Microarchitectural Simulation. IEEE Transactions on Computers, 2013, 62, 705-715.	2.4	14

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19	Thermal Modeling and Validation of a Real-World Mobile AP. IEEE Design and Test, 2018, 35, 55-62.	1.1	14
20	Quantifying the Impact of Monolithic 3D (M3D) Integration on L1 Caches. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 854-865.	3.2	14
21	Signal Strength-Aware Adaptive Offloading with Local Image Preprocessing for Energy Efficient Mobile Devices. IEEE Transactions on Computers, 2020, 69, 99-111.	2.4	13
22	On-Demand Mobile CPU Cooling With Thin-Film Thermoelectric Array. IEEE Micro, 2021, 41, 67-73.	1.8	12
23	On-Demand Solution to Minimize I-Cache Leakage Energy with Maintaining Performance. IEEE Transactions on Computers, 2008, 57, 7-24.	2.4	11
24	Leveraging Process Variation for Performance and Energy: In the Perspective of Overclocking. IEEE Transactions on Computers, 2014, 63, 1316-1322.	2.4	11
25	Fine-Grain Voltage Tuned Cache Architecture for Yield Management Under Process Variations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1532-1536.	2.1	10
26	Energy and Performance Optimization of Demand Paging With OneNAND Flash. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1969-1982.	1.9	8
27	An Energy-Efficient Last-Level Cache Architecture for Process Variation-Tolerant 3D Microprocessors. IEEE Transactions on Computers, 2015, 64, 2460-2475.	2.4	8
28	A novel warp scheduling scheme considering long-latency operations for high-performance GPUs. Journal of Supercomputing, 2020, 76, 3043-3062.	2.4	8
29	Memory streaming acceleration for embedded systems with CPU-accelerator cooperative data processing. Microprocessors and Microsystems, 2019, 71, 102897.	1.8	7
30	Towards refresh-optimized EDRAM-based caches with a selective fine-grain round-robin refresh scheme. Microprocessors and Microsystems, 2017, 49, 95-104.	1.8	6
31	Enhancing Matrix Multiplication With a Monolithic 3-D-Based Scratchpad Memory. IEEE Embedded Systems Letters, 2021, 13, 57-60.	1.3	6
32	PP-cache: A partitioned power-aware instruction cache architecture. Microprocessors and Microsystems, 2006, 30, 268-279.	1.8	5
33	Signal strength-aware adaptive offloading for energy efficient mobile devices. , 2017, , .		5
34	Thermal-aware adaptive VM allocation considering server locations in heterogeneous data centers. Journal of Systems Architecture, 2021, 117, 102071.	2.5	5
35	Sim-ARM1136: A case study on the accuracy of the cycle-accurate simulator. Microprocessors and Microsystems, 2006, 30, 137-144.	1.8	4
36	Temperature-aware Adaptive VM Allocation in Heterogeneous Data Centers. , 2019, , .		4

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37	Monolithic 3D stacked multiply-accumulate units. The Integration VLSI Journal, 2021, 76, 183-189.	1.3	4
38	Quant-PIM: An Energy-Efficient Processing-in-Memory Accelerator for Layerwise Quantized Neural Networks. IEEE Embedded Systems Letters, 2021, 13, 162-165.	1.3	4
39	An Accurate and Energy-Efficient Way Determination Technique for Instruction Caches by Early Tab Matching. , 2008, , .		3
40	Improving the System-on-a-Chip Performance for Mobile Systems by Using Efficient Bus Interface. , 2009, , .		3
41	Exploration of temperature-aware refresh schemes for 3D stacked eDRAM caches. Microprocessors and Microsystems, 2016, 42, 100-112.	1.8	3
42	A System-Level Exploration of Binary Neural Network Accelerators with Monolithic 3D Based Compute-in-Memory SRAM. Electronics (Switzerland), 2021, 10, 623.	1.8	3
43	A Power-Aware Branch Predictor by Accessing the BTB Selectively. Journal of Computer Science and Technology, 2005, 20, 607-614.	0.9	2
44	A SPLIT L2 DATA CACHE FOR SCALABLE CC-NUMA MULTIPROCESSORS. Journal of Circuits, Systems and Computers, 2005, 14, 605-617.	1.0	2
45	Energy-Effective Instruction Fetch Unit for Embedded Processors. , 2008, , .		2
46	Adopting the Banked Register File Scheme for Better Performance and Less Leakage. ETRI Journal, 2008, 30, 624-626.	1.2	2
47	Performance and cache access time of SRAM-eDRAM hybrid caches considering wire delay. , 2013, , .		2
48	A High-Performance Processing-in-Memory Accelerator for Inline Data Deduplication. , 2019, , .		2
49	Characterizing the Thermal Feasibility of Monolithic 3D Microprocessors. IEEE Access, 2021, 9, 120715-120729.	2.6	2
50	A Trace Cache with DVFS Techniques for a Low Power Microprocessor. , 2008, , .		1
51	Exploiting narrow-width values for thermal-aware register file designs. , 2009, , .		1
52	Display Power Management That Detects User Intent. Computer, 2011, 44, 60-66.	1.2	1
53	Distance-aware L2 cache organizations for scalable multiprocessor systems. Journal of Systems Architecture, 2005, 51, 368-381.	2.5	0
54	A fast and simple system performance emulator for enhanced solid state disks: a case study of long read operations. Journal of Zhejiang University: Science C, 2010, 11, 418-424.	0.7	0

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55	Process variation-tolerant 3D microprocessor design: An efficient architectural solution. , 2013, , .		0
56	Do You Waste Laptop Battery to Light the Room?. Computer, 2019, , 1-1.	1.2	0
57	IDRA: An In-storage Data Reorganization Accelerator for Multidimensional Databases. IEEE Embedded Systems Letters, 2021, , 1-1.	1.3	0
58	Characterizing the On-chip Temperature of an Off-the-shelf TSV-based 3D Stacked CPU. , 2021, , .		0