## Kai Ming Yang

List of Publications by Year in descending order

Source: https://exaly.com/author-pdf/1656249/publications.pdf

Version: 2024-02-01

1163117 1372567 11 249 8 10 citations h-index g-index papers 11 11 11 115 docs citations times ranked citing authors all docs

#	Article	IF	CITATIONS
1	Fan-Out Panel-Level Packaging of Mini-LED RGB Display. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2021, 11, 739-747.	2.5	8
2	Panel-Level Chip-Scale Package With Multiple Diced Wafers. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 1110-1124.	2.5	7
3	Investigation of Pillar–Concave Structure for Low-Temperature Cu–Cu Direct Bonding in 3-D/2.5-D Heterogeneous Integration. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 1296-1303.	2.5	5
4	Panel-Level Fan-Out RDL-First Packaging for Heterogeneous Integration. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 1125-1137.	2.5	21
5	Non-Planarization Cu-Cu Direct Bonding and Gang Bonding with Low Temperature and Short Duration in Ambient Atmosphere. , 2019, , .		3
6	Design, Materials, Process, Fabrication, and Reliability of Fan-Out Wafer-Level Packaging. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2018, 8, 991-1002.	2.5	71
7	Fan-Out Wafer-Level Packaging for Heterogeneous Integration. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2018, 8, 1544-1560.	2.5	46
8	Chip-First Fan-Out Panel-Level Packaging for Heterogeneous Integration. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2018, 8, 1561-1572.	2.5	23
9	Design, Materials, Process, and Fabrication of Fan-Out Panel-Level Heterogeneous Integration. Journal of Microelectronics and Electronic Packaging, 2018, 15, 141-147.	0.7	24
10	Low-Temperature Cu–Cu Direct Bonding Using Pillar–Concave Structure in Advanced 3-D Heterogeneous Integration. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2017, 7, 1560-1566.	2.5	13
11	Fan-Out Wafer-Level Packaging (FOWLP) of Large Chip with Multiple Redistribution Layers (RDLs). Journal of Microelectronics and Electronic Packaging, 2017, 14, 123-131.	0.7	28