

Hechen Wang

List of Publications by Year in descending order

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#	ARTICLE	IF	CITATIONS
1	A Digital Root Based Modular Reduction Technique for Power Efficient, Fault Tolerance in FPGAs. , 2020, , .		0
2	Sub-Sampling Direct RF-to-Digital Converter With 1024-APSK Modulation for High Throughput Polar Receiver. IEEE Journal of Solid-State Circuits, 2020, 55, 1064-1076.	5.4	10
3	A 280MS/s 12b SAR-Assisted Hybrid ADC with Time Domain Sub-Range Quantizer in 45nm CMOS. , 2019, , .		14
4	An 8-bit 80-MS/s Fully Self-Timed SAR ADC with 3/2 Interleaved Comparators and High-Order PVT Stabilized HBT Bandgap Reference. , 2019, , .		3
5	A 3.8 mW Sub-Sampling Direct RF-to-Digital Converter for Polar Receiver Achieving 1.94 Gb/s Data Rate with 1024-APSK Modulation. , 2019, , .		1
6	A Reconfigurable Vernier Time-to-Digital Converter With 2-D Spiral Comparator Array and Second-Order $\Delta\Sigma$ Linearization. IEEE Journal of Solid-State Circuits, 2018, 53, 738-749.	5.4	29
7	A bidirectional lens-free digital-bits-in/-out 0.57mm ² terahertz nano-radio in CMOS with 49.3mW Peak power consumption supporting 50cm Internet-of-Things communication. , 2018, , .		3
8	An 802.11a/b/g/n Digital Fractional- N PLL With Automatic TDC Linearity Calibration for Spur Cancellation. IEEE Journal of Solid-State Circuits, 2017, 52, 1210-1220.	5.4	27
9	A bidirectional lens-free digital-bits-in/-out 0.57mm ² Terahertz nano-radio in CMOS with 49.3mW peak power consumption supporting 50cm Internet-of-Things communication. , 2017, , .		11
10	A 330 μ W 1.25ps 400fs-INL vernier time-to-digital converter with 2D reconfigurable spiral arbiter array and 2nd-order $\Delta\Sigma$ linearization. , 2017, , .		1
11	A 14-Bit, 1-ps resolution, two-step ring and 2D Vernier TDC in 130nm CMOS technology. , 2017, , .		16
12	An 802.11 a/b/g/n digital fractional-N PLL with automatic TDC linearity calibration for spur cancellation. , 2016, , .		7
13	A wide tuning triple-band frequency generator MMIC in 0.18 μ m SiGe BiCMOS technology. , 2014, , .		0