Hechen Wang

List of Publications by Year
in descending order

13 papers	122 citations	2258059 3 h-index	2550090 3 g-index
13 all docs	13 docs citations	13 times ranked	186 citing authors

#	Article	IF	Citations
1	A Reconfigurable Vernier Time-to-Digital Converter With 2-D Spiral Comparator Array and Second-Order $Delta Sigma$ Linearization. IEEE Journal of Solid-State Circuits, 2018, 53, 738-749.	5.4	29
2	An 802.11a/b/g/n Digital Fractional- N PLL With Automatic TDC Linearity Calibration for Spur Cancellation. IEEE Journal of Solid-State Circuits, 2017, 52, 1210-1220.	5.4	27
3	A 14-Bit, 1-ps resolution, two-step ring and 2D Vernier TDC in 130nm CMOS technology. , 2017, , .		16
4	A 280MS/s 12b SAR-Assisted Hybrid ADC with Time Domain Sub-Range Quantizer in 45nm CMOS. , 2019, , .		14
5	A bidirectional lens-free digital-bits-in/-out 0.57mm² Terahertz nano-radio in CMOS with 49.3mW peak power consumption supporting 50cm Internet-of-Things communication. , 2017, , .		11
6	Sub-Sampling Direct RF-to-Digital Converter With 1024-APSK Modulation for High Throughput Polar Receiver. IEEE Journal of Solid-State Circuits, 2020, 55, 1064-1076.	5.4	10
7	An 802.11 a/b/g/n digital fractional-N PLL with automatic TDC linearity calibration for spur cancellation. , 2016, , .		7
8	A bidirectional lens-free digital-bits-in/-out 0.57mm2 terahertz nano-radio in CMOS with 49.3mW Peak power consumption supporting 50cm Internet-of-Things communication. , 2018, , .		3
9	An 8-bit 80-MS/s Fully Self-Timed SAR ADC with 3/2 Interleaved Comparators and High-Order PVT Stabilized HBT Bandgap Reference. , 2019, , .		3
10	A 330Î¼W 1.25ps 400fs-INL vernier time-to-digital converter with 2D reconfigurable spiral arbiter array and 2nd-order Î”Î£ linearization. , 2017, , .		1
11	A 3.8 mW Sub-Sampling Direct RF-to-Digital Converter for Polar Receiver Achieving 1.94 Gb/s Data Rate with 1024-APSK Modulation. , 2019, , .		1
12	A wide tuning triple-band frequency generator MMIC in 0.18μm SiGe BiCMOS technology. , 2014, , .		0
13	A Digital Root Based Modular Reduction Technique for Power Efficient, Fault Tolerance in FPGAs. , 2020, , .		0