

# Kaustav Banerjee

## List of Publications by Year in descending order

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153  
papers

12,440  
citations

61687

45  
h-index

42259

96  
g-index

157  
all docs

157  
docs citations

157  
times ranked

14941  
citing authors

#	ARTICLE	IF	CITATIONS
1	Electrical contacts to two-dimensional semiconductors. <i>Nature Materials</i> , 2015, 14, 1195-1205.	13.3	1,318
2	MoS <sub>2</sub> Field-Effect Transistor for Next-Generation Label-Free Biosensors. <i>ACS Nano</i> , 2014, 8, 3992-4003.	7.3	870
3	Role of Metal Contacts in Designing High-Performance Monolayer n-Type WSe <sub>2</sub> Field Effect Transistors. <i>Nano Letters</i> , 2013, 13, 1983-1990.	4.5	833
4	A subthermionic tunnel field-effect transistor with an atomically thin channel. <i>Nature</i> , 2015, 526, 91-95.	13.7	793
5	Computational Study of Metal Contacts to Monolayer Transition-Metal Dichalcogenide Semiconductors. <i>Physical Review X</i> , 2014, 4, .	2.8	429
6	Carbon Nanomaterials for Next-Generation Interconnects and Passives: Physics, Status, and Prospects. <i>IEEE Transactions on Electron Devices</i> , 2009, 56, 1799-1821.	1.6	390
7	Two-dimensional van der Waals materials. <i>Physics Today</i> , 2016, 69, 38-44.	0.3	381
8	Modeling, Analysis, and Design of Graphene Nano-Ribbon Interconnects. <i>IEEE Transactions on Electron Devices</i> , 2009, 56, 1567-1578.	1.6	329
9	Functionalization of Transition Metal Dichalcogenides with Metallic Nanoparticles: Implications for Doping and Gas-Sensing. <i>Nano Letters</i> , 2015, 15, 2852-2862.	4.5	329
10	Circuit Modeling and Performance Analysis of Multi-Walled Carbon Nanotube Interconnects. <i>IEEE Transactions on Electron Devices</i> , 2008, 55, 1328-1337.	1.6	324
11	Steep Subthreshold Slope n- and p-Type Tunnel-FET Devices for Low-Power and Energy-Efficient Digital Circuits. <i>IEEE Transactions on Electron Devices</i> , 2009, 56, 2752-2761.	1.6	314
12	High-performance MoS <sub>2</sub> transistors with low-resistance molybdenum contacts. <i>Applied Physics Letters</i> , 2014, 104, .	1.5	312
13	Vertical Si-Nanowire $\text{Si}^{\text{nanowire}}$ Tunneling FETs With Low Subthreshold Swing		

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19	CMOS-Compatible Vertical-Silicon-Nanowire Gate-All-Around p-Type Tunneling FETs With $50\text{ mV/decade}$ Subthreshold Swing. IEEE Electron Device Letters, 2011, 32, 1504-1506.	2.2	158
20	On the Applicability of Single-Walled Carbon Nanotubes as VLSI Interconnects. IEEE Nanotechnology Magazine, 2009, 8, 542-559.	1.1	156
21	Grain-Orientation Induced Work Function Variation in Nanoscale Metal-Gate Transistorsâ€”Part I: Modeling, Analysis, and Experimental Validation. IEEE Transactions on Electron Devices, 2010, 57, 2504-2514.	1.6	156
22	High-Frequency Analysis of Carbon Nanotube Interconnects and Implications for On-Chip Inductor Design. IEEE Transactions on Electron Devices, 2009, 56, 2202-2214.	1.6	144
23	Impact of Contact on the Operation and Performance of Back-Gated Monolayer $\text{MoS}_2$ Field-Effect-Transistors. ACS Nano, 2015, 9, 7904-7912.	7.3	137
24	Controllable and Rapid Synthesis of High-Quality and Large-Area Bernal Stacked Bilayer Graphene Using Chemical Vapor Deposition. Chemistry of Materials, 2014, 26, 907-915.	3.2	135
25	A Compact Currentâ€”Voltage Model for 2D Semiconductor Based Field-Effect Transistors Considering Interface Traps, Mobility Degradation, and Inefficient Doping Effect. IEEE Transactions on Electron Devices, 2014, 61, 4282-4290.	1.6	133
26	A thermally-aware performance analysis of vertically integrated (3-D) processor-memory hierarchy. , 2006, , .		127
27	Cool Chips: Opportunities and Implications for Power and Thermal Management. IEEE Transactions on Electron Devices, 2008, 55, 245-255.	1.6	115
28	Intercalation Doped Multilayer-Graphene-Nanoribbons for Next-Generation Interconnects. Nano Letters, 2017, 17, 1482-1488.	4.5	110
29	Intimate contacts. Nature Materials, 2014, 13, 1076-1078.	13.3	107
30	Defect and strain engineering of monolayer $\text{WSe}_2$ enables site-controlled single-photon emission up to $150\text{ K}$ . Nature Communications, 2021, 12, 3585.	5.8	105
31	Is negative capacitance FET a steep-slope logic switch?. Nature Communications, 2020, 11, 196.	5.8	91
32	Low-Frequency Noise in Bilayer $\text{MoS}_2$ Transistor. ACS Nano, 2014, 8, 5633-5640.	7.3	89
33	On thermal effects in deep sub-micron VLSI interconnects. , 1999, , .		80
34	Grain-Orientation Induced Work Function Variation in Nanoscale Metal-Gate Transistorsâ€”Part II: Implications for Process, Device, and Circuit Design. IEEE Transactions on Electron Devices, 2010, 57, 2515-2525.	1.6	78
35	On-chip intercalated-graphene inductors for next-generation radio frequency electronics. Nature Electronics, 2018, 1, 46-51.	13.1	77
36	Ultimate Monolithic-3D Integration With 2D Materials: Rationale, Prospects, and Challenges. IEEE Journal of the Electron Devices Society, 2019, 7, 878-887.	1.2	77

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37	Carbon Nanomaterials: The Ideal Interconnect Technology for Next-Generation ICs. IEEE Design and Test of Computers, 2010, 27, 20-31.	1.4	75
38	2-D Layered Materials for Next-Generation Electronics: Opportunities and Challenges. IEEE Transactions on Electron Devices, 2018, 65, 4109-4121.	1.6	74
39	Fundamental limitations of conventional-FET biosensors: Quantum-mechanical-tunneling to the rescue. , 2012, , .		73
40	Interconnect challenges for nanoscale electronic circuits. Jom, 2004, 56, 30-31.	0.9	69
41	High-Frequency Behavior of Graphene-Based Interconnectsâ€™Part I: Impedance Modeling. IEEE Transactions on Electron Devices, 2011, 58, 843-852.	1.6	65
42	Metal-to-Multilayer-Graphene Contactâ€™Part I: Contact Resistance Modeling. IEEE Transactions on Electron Devices, 2012, 59, 2444-2452.	1.6	62
43	A Novel Variation-Tolerant Keeper Architecture for High-Performance Low-Power Wide Fan-In Dynamic or Gates. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1567-1577.	2.1	60
44	Proposal for all-graphene monolithic logic circuits. Applied Physics Letters, 2013, 103, .	1.5	60
45	Tunnel-field-effect-transistor based gas-sensor: Introducing gas detection with a quantum-mechanical transducer. Applied Physics Letters, 2013, 102, .	1.5	59
46	Analytical Thermal Model for Self-Heating in Advanced FinFET Devices With Implications for Design and Reliability. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1045-1058.	1.9	57
47	Statistical modeling of metal-gate Work-Function Variability in emerging device technologies and implications for circuit design. , 2008, , .		56
48	Subthreshold-swing physics of tunnel field-effect transistors. AIP Advances, 2014, 4, .	0.6	54
49	High-performance few-layer-MoS<sub>2</sub>/inf&gt; field-effect-transistor with record low contact-resistance. , 2013, , .		52
50	High-Frequency Behavior of Graphene-Based Interconnectsâ€™Part II: Impedance Analysis and Implications for Inductor Design. IEEE Transactions on Electron Devices, 2011, 58, 853-859.	1.6	50
51	Current Status and Future Perspectives of Carbon Nanotube Interconnects. , 2008, , .		45
52	A Statistical Framework for Estimation of Full-Chip Leakage-Power Distribution Under Parameter Variations. IEEE Transactions on Electron Devices, 2007, 54, 2930-2945.	1.6	41
53	Boosting Hydrogen Evolution Performance of MoS<sub>2</sub> by Band Structure Engineering. Advanced Materials Interfaces, 2017, 4, 1700303.	1.9	40
54	Analysis of non-uniform temperature-dependent interconnect performance in high performance ICs. , 2001, , .		39

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55	A computational study of metal-contacts to beyond-graphene 2D semiconductor materials. , 2012, , .		38
56	Can 2D-Nanocrystals Extend the Lifetime of Floating-Gate Transistor Based Nonvolatile Memory?. IEEE Transactions on Electron Devices, 2014, 61, 3456-3464.	1.6	38
57	Electron-hole duality during band-to-band tunneling process in graphene-nanoribbon tunnel-field-effect-transistors. Applied Physics Letters, 2010, 97, .	1.5	37
58	Graphene and beyond-graphene 2D crystals for next-generation green electronics. Proceedings of SPIE, 2014, , .	0.8	37
59	Graphene nano-ribbon (GNR) interconnects: A genuine contender or a delusive dream?. , 2008, , .		36
60	Compact Modeling and Analysis of Through-Si-Via-Induced Electrical Noise Coupling in Three-Dimensional ICs. IEEE Transactions on Electron Devices, 2011, 58, 4024-4034.	1.6	34
61	Modeling and Analysis of Self-Heating in FinFET Devices for Improved Circuit and EOS/ESD Performance. , 2007, , .		33
62	One-Dimensional Edge Contacts to Two-Dimensional Transition-Metal Dichalcogenides: Uncovering the Role of Schottky-Barrier Anisotropy in Charge Transport across $MoS_2/Metal$ Interfaces. Physical Review Applied, 2021, 15, .	1.5	33
63	Carbon Nanotube Vias: Does Ballistic Electronâ€“Phonon Transport Imply Improved Performance and Reliability?. IEEE Transactions on Electron Devices, 2011, 58, 2689-2701.	1.6	31
64	Metal-to-Multilayer-Graphene Contactâ€“Part II: Analysis of Contact Resistance. IEEE Transactions on Electron Devices, 2012, 59, 2453-2460.	1.6	31
65	An Ultra-Short Channel Monolayer $MoS_2$ FET Defined By the Curvature of a Thin Nanowire. IEEE Electron Device Letters, 2016, 37, 1497-1500.	2.2	31
66	A Novel Enhanced Electric-Field Impact-Ionization MOS Transistor. IEEE Electron Device Letters, 2010, 31, 1175-1177.	2.2	30
67	Graphene nanoribbon based negative resistance device for ultra-low voltage digital logic applications. Applied Physics Letters, 2013, 102, 043114.	1.5	30
68	Design Optimization of FinFET Domino Logic Considering the Width Quantization Property. IEEE Transactions on Electron Devices, 2010, 57, 2934-2943.	1.6	29
69	Accurate Intrinsic Gate Capacitance Model for Carbon Nanotube-Array Based FETs Considering Screening Effect. IEEE Electron Device Letters, 2008, 29, 1408-1411.	2.2	28
70	Scaling Analysis of On-Chip Power Grid Voltage Variations in Nanometer Scale ULSI. Analog Integrated Circuits and Signal Processing, 2005, 42, 277-290.	0.9	27
71	Vertically Stacked and Independently Controlled Twin-Gate MOSFETs on a Single Si Nanowire. IEEE Electron Device Letters, 2011, 32, 1492-1494.	2.2	27
72	Low-Resistivity Long-Length Horizontal Carbon Nanotube Bundles for Interconnect Applicationsâ€“Part I: Process Development. IEEE Transactions on Electron Devices, 2013, 60, 2862-2869.	1.6	25

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73	Characterization of FeCl <sub>3</sub> Intercalation Doped CVD Few-Layer Graphene. IEEE Electron Device Letters, 2016, 37, 1246-1249.	2.2	25
74	Compact AC modeling and analysis of Cu, W, and CNT based through-silicon vias (TSVs) in 3-D ICs. , 2009, , .		24
75	A Fully Analytical Model for the Series Impedance of Through-Silicon Vias With Consideration of Substrate Effects and Coupling With Horizontal Interconnects. IEEE Transactions on Electron Devices, 2011, 58, 3529-3540.	1.6	23
76	On the Electrostatic Discharge Robustness of Graphene. IEEE Transactions on Electron Devices, 2014, 61, 1920-1928.	1.6	22
77	0.5T0.5Râ€”An Ultracompact RRAM Cell Uniquely Enabled by van der Waals Heterostructures. IEEE Transactions on Electron Devices, 2021, 68, 2033-2040.	1.6	22
78	Quantumâ€”Engineered Devices Based on 2D Materials for Nextâ€”Generation Information Processing and Storage. Advanced Materials, 2023, 35, e2109894.	11.1	22
79	Impact-ionization field-effect-transistor based biosensors for ultra-sensitive detection of biomolecules. Applied Physics Letters, 2013, 102, .	1.5	21
80	CMOS-Compatible Doped-Multilayer-Graphene Interconnects for Next-Generation VLSI. , 2018, , .		21
81	Performance evaluation and design considerations of 2D semiconductor based FETs for sub-10 nm VLSI. , 2014, , .		20
82	Characterization of self-heating and current-carrying capacity of intercalation doped graphene-nanoribbon interconnects. , 2017, , .		19
83	Designing band-to-band tunneling field-effect transistors with 2D semiconductors for next-generation low-power VLSI. , 2015, , .		18
84	High-frequency effects in carbon nanotube interconnects and implications for on-chip inductor design. , 2008, , .		17
85	Aging-resilient design of pipelined architectures using novel detection and correction circuits. , 2010, , .		17
86	2D electronics: Graphene and beyond. , 2013, , .		17
87	Low-Resistivity Long-Length Horizontal Carbon Nanotube Bundles for Interconnect Applicationsâ€”Part II: Characterization. IEEE Transactions on Electron Devices, 2013, 60, 2870-2876.	1.6	16
88	Designing artificial 2D crystals with site and size controlled quantum dots. Scientific Reports, 2017, 7, 9965.	1.6	16
89	A Self-Consistent Substrate Thermal Profile Estimation Technique for Nanoscale ICsâ€”Part I: Electrothermal Couplings and Full-Chip Package Thermal Model. IEEE Transactions on Electron Devices, 2007, 54, 3342-3350.	1.6	14
90	Effect of band-tails on the subthreshold performance of 2D tunnel-FETs. , 2016, , .		14

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91	Undoped and catalyst-free germanium nanowires for high-performance p-type enhancement-mode field-effect transistors. <i>Journal of Materials Chemistry C</i> , 2016, 4, 5102-5108.	2.7	14
92	Area-Selective-CVD Technology Enabled Top-Gated and Scalable 2D-Heterojunction Transistors with Dynamically Tunable Schottky Barrier. , 2019, , .		14
93	A Self-Consistent Substrate Thermal Profile Estimation Technique for Nanoscale ICsâ€”Part II: Implementation and Implications for Power Estimation and Thermal Management. <i>IEEE Transactions on Electron Devices</i> , 2007, 54, 3351-3360.	1.6	13
94	A Design-Specific and Thermally-Aware Methodology for Trading-Off Power and Performance in Leakage-Dominant CMOS Technologies. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2008, 16, 1488-1498.	2.1	13
95	Compact modeling and analysis of coupling noise induced by through-Si-vias in 3-D ICs. , 2010, , .		13
96	Understanding the Device Physics in Polymerâ€”Based Ionicâ€”Organic Ratchets. <i>Advanced Materials</i> , 2017, 29, 1606464.	11.1	12
97	All-carbon interconnect scheme integrating graphene-wires and carbon-nanotube-vias. , 2017, , .		12
98	Graphene inductors for high-frequency applications - design, fabrication, characterization, and study of skin effect. , 2014, , .		11
99	Mechanisms leading to erratic snapback behavior in bipolar junction transistors with base emitter shorted. <i>Journal of Applied Physics</i> , 2005, 97, 084504.	1.1	10
100	Top illuminated inverted organic ultraviolet photosensors with single layer graphene electrodes. <i>Applied Physics Letters</i> , 2012, 101, 033302.	1.5	10
101	Engineered 2D nanomaterialsâ€”protein interfaces for efficient sensors. <i>Journal of Materials Research</i> , 2015, 30, 3565-3574.	1.2	10
102	Demonstration of CMOS-Compatible Multi-Level Graphene Interconnects With Metal Vias. <i>IEEE Transactions on Electron Devices</i> , 2021, 68, 2083-2091.	1.6	10
103	Graphene based heterostructure tunnel-FETs for low-voltage/high-performance ICs. , 2010, , .		9
104	A mode-balanced reconfigurable logic gate built in a van der Waals strata. <i>Npj 2D Materials and Applications</i> , 2021, 5, .	3.9	9
105	Thermal Challenges of 3D ICs. <i>Integrated Circuits and Systems</i> , 2008, , 1-26.	0.2	8
106	Physical Modeling of the Capacitance and Capacitive Coupling Noise of Through-Oxide Vias in FDSOI-Based Ultra-High Density 3-D ICs. <i>IEEE Transactions on Electron Devices</i> , 2013, 60, 123-131.	1.6	8
107	Monolithic-3D Integration with 2D Materials: Toward Ultimate Vertically-Scaled 3D-ICs. , 2018, , .		8
108	Impact of Transport Anisotropy on the Performance of van der Waals Materials-Based Electron Devices. <i>IEEE Transactions on Electron Devices</i> , 2020, 67, 1310-1316.	1.6	8

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109	Two-dimensional materials enabled next-generation low-energy compute and connectivity. MRS Bulletin, 2021, 46, 1211-1228.	1.7	8
110	Metallic-nanoparticle assisted enhanced band-to-band tunneling current. Applied Physics Letters, 2011, 99, 133116.	1.5	7
111	Prospects of graphene electrodes in photovoltaics. , 2013, , .		7
112	An Electrothermally-Aware Full-Chip Substrate Temperature Gradient Evaluation Methodology for Leakage Dominant Technologies with Implications for Power Estimation and Hot-Spot Management. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	6
113	Carbon Nanotube Vias: A Reality Check. , 2007, , .		6
114	Scaling analysis of graphene nanoribbon tunnel-FETs. , 2009, , .		6
115	Can Carbon Nanotubes Extend the Lifetime of On-Chip Electrical Interconnections?. , 2006, , .		5
116	3D device modeling of damage due to filamentation under an ESD event in nanometer scale drain extended NMOS (DE-NMOS). , 2008, , .		5
117	Analytical Expressions for High-Frequency VLSI Interconnect Impedance Extraction in the Presence of a Multilayer Conductive Substrate. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1047-1060.	1.9	5
118	Prospects of carbon nanomaterials for next-generation green electronics. , 2010, , .		5
119	Fast extraction of high-frequency parallel admittance of Through-Silicon-Vias and their capacitive coupling-noise to active regions. , 2012, , .		5
120	A Compact Current-Voltage Model for 2-D-Semiconductor-Based Lateral Homo-/Hetero-Junction Tunnel-FETs. IEEE Transactions on Electron Devices, 2020, 67, 4473-4481.	1.6	5
121	High-speed low-power FinFET based domino logic. , 2009, , .		4
122	Effect of Grain Orientation on NBTI Variation and Recovery in Emerging Metal-Gate Devices. IEEE Electron Device Letters, 2010, 31, 794-796.	2.2	4
123	Work-function variation induced fluctuation in bias-temperature-instability characteristics of emerging metal-gate devices and implications for digital design. , 2010, , .		4
124	A built-in aging detection and compensation technique for improving reliability of nanoscale CMOS designs. , 2010, , .		4
125	(Invited) 2D/3D Tunnel-FET: Toward Green Transistors and Sensors. ECS Transactions, 2017, 77, 185-189.	0.3	4
126	Room temperature 2D memristive transistor with optical short-term plasticity. , 2017, , .		4



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127	Computational study of gate-induced drain leakage in 2D-semiconductor field-effect transistors. , 2017, , .		4
128	Interfacial Thermal Conductivity of 2D Layered Materials: An Atomistic Approach. , 2018, , .		4
129	An Interconnect Scaling Scheme with Constant On-Chip Inductive Effects. Analog Integrated Circuits and Signal Processing, 2003, 35, 97-105.	0.9	3
130	Prospects of ultra-thin nanowire gated 2D-FETs for next-generation CMOS technology. , 2016, , .		3
131	Irradiation of Nanostrained Monolayer WSe <sub>2</sub> for Site-Controlled Single-Photon Emission up to 150K. , 2020, , .		3
132	0.5T0.5R - Introducing an Ultra-Compact Memory Cell Enabled by Shared Graphene Edge-Contact and h-BN Insulator. , 2020, , .		3
133	High-Frequency Mutual Impedance Extraction of VLSI Interconnects In the Presence of a Multi-layer Conducting Substrate. , 2008, , .		2
134	Impact of strain engineering and channel orientation on the ESD performance of nanometer scale CMOS devices. , 2009, , .		2
135	AC conductance modeling and analysis of graphene nanoribbon interconnects. , 2010, , .		2
136	On the Electrostatics of Bernal-Stacked Few-Layer Graphene on Surface-Passivated Semiconductors. IEEE Nanotechnology Magazine, 2014, 13, 94-100.	1.1	2
137	Performance analysis of multi-walled carbon nanotube based interconnects. , 2007, , .		1
138	Modeling and analysis of intrinsic gate capacitance for carbon nanotube array based devices considering variation in screening effect and diameter. , 2007, , .		1
139	A quantitative inquisition into ESD sensitivity to strain in nanoscale CMOS protection devices. , 2010, , .		1
140	Compact capacitance and capacitive coupling-noise modeling of Through-Oxide Vias in FDSOI based ultra-high density 3-D ICs. , 2011, , .		1
141	Some Clarifications on "Compact Modeling and Analysis of Through-Si-Via Induced Electrical Noise Coupling in Three-Dimensional ICs" IEEE Transactions on Electron Devices, 2012, 59, 2861-2862.	1.6	1
142	NanoCarbon for next-generation green electronics: Status and prospects. , 2013, , .		1
143	How to derive the highest mobility from 2D FETs " A first-principle study. , 2017, , .		1
144	Can Kinetic Inductance in Low-Dimensional Materials Enable a New Generation of RF-Electronics?. , 2018, , .		1

#	ARTICLE	IF	CITATIONS
145	2D Materials for Smart Life. , 2018, , .		1
146	A fast semi-numerical technique for the solution of the poisson-boltzmann equation in a cylindrical nanowire. , 2007, , .		0
147	2-Dimensional tunnel devices and circuits on graphene: Opportunities and challenges. , 2013, , .		0
148	Novel logic devices based on 2D crystal semiconductors: Opportunities and challenges. , 2013, , .		0
149	Electrical characterization of back-gated and top-gated germanium-core/silicon-shell nanowire field-effect transistors. , 2016, , .		0
150	Computational Study of Spin Injection in 2D Materials. , 2019, , .		0
151	Correction to "Analytical Thermal Model for Self-Heating in Advanced FinFET Devices With Implications for Design and Reliability" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 277-277.	1.9	0
152	NEMS-Based Ultra Energy-Efficient Digital ICs: Materials, Device Architectures, Logic Implementation, and Manufacturability. , 2017, , 245-276.		0
153	Reliability and Performance of CMOS-Compatible Multi-Level Graphene Interconnects Incorporating Vias. , 2020, , .		0