Weiqiang Liu

List of Publications by Year in Descending Order

121 papers	1,328 citations	18 h-index	30 g-index
146 ext. papers	1,982 ext. citations	3.1 avg, IF	5.37 L-index

#	Paper	IF	Citations
121	Ultra High-Speed Polynomial Multiplications for Lattice-based Cryptography on FPGAs. *IEEE Transactions on Emerging Topics in Computing*, **2022**, 1-1	4.1	3
120	Design of Majority Logic-based Approximate Booth Multipliers for Error-Tolerant Applications. *IEEE Nanotechnology Magazine*, **2022**, 1-1	2.6	1
119	Low-Power Approximate RPR Scheme for Unsigned Integer Arithmetic Computation. *IEEE Open Journal of Nanotechnology*, **2022**, 3, 36-44	2.1	
118	A High-Performance SIKE Hardware Accelerator. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2022**, 1-13	2.6	3
117	Design and analysis of hardware Trojans in approximate circuits. *Electronics Letters*, **2022**, 58, 197-199	1.1	
116	PTB: Robust Physical Backdoor Attacks against Deep Neural Networks in Real World. *Computers and Security*, **2022**, 102726	4.9	1
115	Security and Approximation: Vulnerabilities in Approximation-aware Testing. *IEEE Transactions on Emerging Topics in Computing*, **2022**, 1-1	4.1	
114	Detect and Remove Watermark in Deep Neural Networks via Generative Adversarial Networks. *Lecture Notes in Computer Science*, **2021**, 341-357	0.9	1
113	Precision Adaptive MFCC Based on R2SDF-FFT and Approximate Computing for Low-Power Speech Keywords Recognition. *IEEE Circuits and Systems Magazine*, **2021**, 21, 24-39	3.2	5
112	Intellectual Property Protection for Deep Learning Models: Taxonomy, Methods, Attacks, and Evaluations. *IEEE Transactions on Artificial Intelligence*, **2021**, 1-1	4.7	1
111	More is Less: Domain-Specific Speech Recognition Microprocessor Using One-Dimensional Convolutional Recurrent Neural Network. *IEEE Transactions on Circuits and Systems I: Regular Papers* , **2021**, 1-12	3.9	2
110	AxRLWE: A Multi-level Approximate Ring-LWE Co-processor for Lightweight IoT Applications. *IEEE Internet of Things Journal*, **2021**, 1-1	10.7	3
109	An Efficient High SFDR PDDS Using High-Pass-Shaped Phase Dithering. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 29, 2003-2007	2.6	
108	A large-scale comprehensive evaluation of single-slice ring oscillator and PicoPUF bit cells on 28-nm Xilinx FPGAs. *Journal of Cryptographic Engineering*, **2021**, 11, 227-238	1.9	3
107	Towards CRYSTALS-Kyber: A M-LWE Cryptoprocessor with Area-Time Trade-Off **2021**,		2
106	. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 68, 1566-1570	3.5	6
105	A Dynamic Highly Reliable SRAM-Based PUF Retaining Memory Function **2021**,		1

104	High-Performance Systolic Array Montgomery Multiplier for SIKE **2021**,		1
103	BCD Adder Designs Based on Three-Input XOR and Majority Gates. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 68, 1942-1946	3.5	3
102	A Modeling Attack Resistant Deception Technique for Securing Lightweight-PUF-Based Authentication. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 1183-1196	2.5	17
101	AxSA: On the Design of High-Performance and Power-Efficient Approximate Systolic Arrays for Matrix Multiplication. *Journal of Signal Processing Systems*, **2021**, 93, 605-615	1.4	2
100	. *IEEE Transactions on Emerging Topics in Computing*, **2021**, 1-1	4.1	3
99	. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 68, 250-263	3.9	18
98	Background Calibration for Bit Weights in Pipelined ADCs Using Adaptive Dither Windows. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 68, 1783-1787	3.5	2
97	. *IEEE Open Journal of the Computer Society*, **2021**, 2, 38-52	3.6	4
96	Backdoors hidden in facial features: a novel invisible backdoor attack against face recognition systems. *Peer-to-Peer Networking and Applications*, **2021**, 14, 1458-1474	3.1	2
95	. *IEEE Open Journal of Nanotechnology*, **2021**, 2, 31-40	2.1	3
94	A Dynamically Configurable PUF and Dynamic Matching Authentication Protocol. *IEEE Transactions on Emerging Topics in Computing*, **2021**, 1-1	4.1	2
93	Design of An Approximate FFT Processor Based on Approximate Complex Multipliers **2021**,		1
92	A Real-Time Hardware Emulator for 3D Non-Stationary U2V Channels. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 68, 3951-3964	3.9	5
91	A lightweight key renewal scheme based authentication protocol with configurable RO PUF for clustered sensor networks. *Microelectronics Journal*, **2021**, 117, 105265	1.8	4
90	. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 68, 4102-4115	3.9	3
89	. *IEEE Transactions on Information Forensics and Security*, **2021**, 1-1	8	2
88	Ten years of hardware Trojans: a survey from the attackerS perspective. *IET Computers and Digital Techniques*, **2020**, 14, 231-246	0.9	9
87	. *IEEE Transactions on Dependable and Secure Computing*, **2020**, 1-1	3.9	6

86	. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2020**, 67, 4869-4882	3.9	6
85	Lightweight Modeling Attack-Resistant Multiplexer-Based Multi-PUF (MMPUF) Design on FPGA. *Electronics (Switzerland)*, **2020**, 9, 815	2.6	6
84	. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 886-890	3.5	17
83	DPAEG: A Dependency Parse-Based Adversarial Examples Generation Method for Intelligent Q&A Robots. *Security and Communication Networks*, **2020**, 2020, 1-15	1.9	3
82	A Retrospective and Prospective View of Approximate Computing [Point of View}. *Proceedings of the IEEE*, **2020**, 108, 394-399	14.3	54
81	. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2020**, 67, 4707-4718	3.9	4
80	Hybrid Low Radix Encoding-Based Approximate Booth Multipliers. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 3367-3371	3.5	19
79	Background Calibration of Bit Weights in Pipelined-SAR ADCs Using Paired Comparators. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 1074-1078	2.6	7
78	Mathematical Modeling Analysis of Strong Physical Unclonable Functions. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 4426-4438	2.5	8
77	. *IEEE Access*, **2020**, 8, 74720-74742	3.5	33
76	Security in Approximate Computing and Approximate Computing for Security: Challenges and Opportunities. *Proceedings of the IEEE*, **2020**, 108, 2214-2231	14.3	12
75	Security Analysis of Hardware Trojans on Approximate Circuits **2020**,		5
74	Design, evaluation and application of approximate-truncated Booth multipliers. *IET Circuits, Devices and Systems*, **2020**, 14, 1305-1317	1.1	0
73	Active DNN IP Protection: A Novel User Fingerprint Management and DNN Authorization Control Technique **2020**,		3
72	High Performance Modular Multiplication for SIDH. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 3118-3122	2.5	9
71	AxMM: Area and Power Efficient Approximate Modular Multiplier for R-LWE Cryptosystem **2020**,		7
70	. *IEEE Transactions on Sustainable Computing*, **2020**, 1-1	3.5	14
69	Transformer PUF : A Highly Flexible Configurable RO PUF Based on FPGA **2020**,		3

68	A Novel Feature Extraction Strategy for Hardware Trojan Detection **2020**,		6
67	Design and Implementation of an Approximate Softmax Layer for Deep Neural Networks **2020**,		9
66	DC-LSTM: Deep Compressed LSTM with Low Bit-Width and Structured Matrices **2020**,		3
65	Design of Unsigned Approximate Hybrid Dividers based on Restoring Array and Logarithmic Dividers. *IEEE Transactions on Emerging Topics in Computing*, **2020**, 1-1	4.1	1
64	. *Proceedings of the IEEE*, **2020**, 108, 2103-2107	14.3	4
63	Lattice-based Cryptography for IoT in A Quantum World: Are We Ready? **2019**,		10
62	. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 4727-4739	3.9	18
61	. *IEEE Transactions on Emerging Topics in Computing*, **2019**, 1-1	4.1	17
60	Multi-Incentive Delay-Based (MID) PUF **2019**,		1
59	High-performance approximate half and full adder cells using NAND logic gate. *IEICE Electronics Express*, **2019**, 16, 20190043-20190043	0.5	8
58	Optimized Modular Multiplication for Supersingular Isogeny Diffie-Hellman. *IEEE Transactions on Computers*, **2019**, 68, 1249-1255	2.5	14
57	XOR-Based Low-Cost Reconfigurable PUFs for IoT Security. *Transactions on Embedded Computing Systems*, **2019**, 18, 1-21	1.8	18
56	. *IEEE Access*, **2019**, 7, 5124-5140	3.5	14
55	. *IEEE Transactions on Computers*, **2019**, 68, 287-293	2.5	5
54	. *IEEE Transactions on Emerging Topics in Computing*, **2019**, 1-1	4.1	16
53	Optimized Schoolbook Polynomial Multiplication for Compact Lattice-Based Cryptography on FPGA. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 2459-2463	2.6	38
52	Building an accurate hardware Trojan detection technique from inaccurate simulation models and unlabelled ICs. *IET Computers and Digital Techniques*, **2019**, 13, 348-359	0.9	6
51	Theoretical Analysis of Delay-Based PUFs and Design Strategies for Improvement **2019**,		6

50	. *IEEE Transactions on Emerging Topics in Computing*, **2019**, 1-1	4.1	5
49	**2019**,		2
48	Theoretical Analysis of Configurable RO PUFs and Strategies to Enhance Security **2019**,		2
47	A Modeling Attack Resistant Deception Technique for Securing PUF based Authentication **2019**,		12
46	Design and Analysis of Majority Logic Based Approximate Radix-4 Booth Encoders **2019**,		3
45	INA: Incremental Network Approximation Algorithm for Limited Precision Deep Neural Networks **2019**,		4
44	New Majority Gate-Based Parallel BCD Adder Designs for Quantum-Dot Cellular Automata. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2019**, 66, 1232-1236	3.5	10
43	. *IEEE Transactions on Computers*, **2019**, 68, 804-819	2.5	37
42	A machine learning attack resistant multi-PUF design on FPGA **2018**,		23
41	Design and Optimization of Modular Multiplication for SIDH **2018**,		6
40	. *IEEE Transactions on Multi-Scale Computing Systems*, **2018**, 4, 299-312		15
39	Data Compression Device Based on Modified LZ4 Algorithm. *IEEE Transactions on Consumer Electronics*, **2018**, 64, 110-117	4.8	18
38	. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2018**, 65, 2856-2868	3.9	59
37	Design of High-Speed Wide-Word Hybrid Parallel-Prefix/Carry-Select and Skip Adders. *Journal of Signal Processing Systems*, **2018**, 90, 409-419	1.4	5
36	Designs of Approximate Floating-Point Multipliers with Variable Accuracy for Error-Tolerant Applications. *Journal of Signal Processing Systems*, **2018**, 90, 641-654	1.4	7
35	Ultra-Lightweight and Reconfigurable Tristate Inverter Based Physical Unclonable Function Design. *IEEE Access*, **2018**, 6, 28478-28487	3.5	15
34	Design of Approximate FFT with Bit-width Selection Algorithms **2018**,		2
33	**2018**,		16

32	**2018**,		2
31	A Highly Flexible Lightweight and High Speed True Random Number Generator on FPGA **2018**,		4
30	Lightweight Hardware Implementation of R-LWE Lattice-Based Cryptography **2018**,		9
29	Approximate Computing and Its Application to Hardware Security **2018**, 43-67		3
28	A Co-training Based Hardware Trojan Detection Technique by Exploiting Unlabeled ICs and Inaccurate Simulation Models **2018**,		4
27	**2018**,		10
26	Design of Dynamic Range Approximate Logarithmic Multipliers **2018**,		3
25	Design of Approximate Radix-4 Booth Multipliers for Error-Tolerant Computing. *IEEE Transactions on Computers*, **2017**, 66, 1435-1441	2.5	123
24	Algorithm and Design of a Fully Parallel Approximate Coordinate Rotation Digital Computer (CORDIC). *IEEE Transactions on Multi-Scale Computing Systems*, **2017**, 3, 139-151		14
23	. *IEEE Transactions on Computers*, **2017**, 66, 1994-2004	2.5	10
22	Design of Approximate Logarithmic Multipliers **2017**,		7
21	Multiprecision Multiplication on ARMv8 **2017**,		1
20	Design of Approximate High-Radix Dividers by Inexact Binary Signed-Digit Addition **2017**,		14
19	XOR gate based low-cost configurable RO PUF **2017**,		16
18	DC MUX PUF: A highly reliable feed-back MUX PUF based on measuring duty cycle **2017**,		1
17	Notice of Violation of IEEE Publication Principles: Application of LDPC codes on PUF error correction based on code-offset construction **2017**,		1
16	. *IEEE Transactions on Computers*, **2016**, 65, 308-314	2.5	29
15	A Parallel Decimal Multiplier Using Hybrid Binary Coded Decimal (BCD) Codes **2016**,		4

14	Design and Performance Evaluation of Approximate Floating-Point Multipliers **2016**,		10
13	. *IEEE Transactions on Computers*, **2016**, 65, 1165-1171	2.5	22
12	. *IEEE Transactions on Computers*, **2016**, 65, 2522-2533	2.5	33
11	A Reconfigurable Memory PUF Based on Tristate Inverter Arrays **2016**,		2
10	Design of Approximate Unsigned Integer Non-restoring Divider for Inexact Computing **2015**,		29
9	Design of 3-D quantum-dot cellular automata adders. *IEICE Electronics Express*, **2015**, 12, 20150195-20150195	0.5	2
8	A First Step Toward Cost Functions for Quantum-Dot Cellular Automata Designs. *IEEE Nanotechnology Magazine*, **2014**, 13, 476-487	2.6	112
7	Inexact floating-point adder for dynamic image processing **2014**,		10
6	QCA Systolic Array Design. *IEEE Transactions on Computers*, **2013**, 62, 548-560	2.5	45
5	Cost-efficient decimal adder design in Quantum-dot cellular automata **2012**,		8
4	A review of QCA adders and metrics **2012**,		4
3	Montgomery modular multiplier design in quantum-dot cellular automata using cut-set retiming **2010**,		4
2	QCA Systolic Matrix Multiplier **2010**,		17
1	Design and analysis of energy-efficient approximate Booth-folding squarers with precision recovery. *Electronics Letters*,	1.1	