Weiqiang Liu

List of Publications by Year
in descending order

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146	2,712	236833	254106
papers	citations	25 h-index	43 g-index

146	146	146	1307
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Design of Approximate Radix-4 Booth Multipliers for Error-Tolerant Computing. IEEE Transactions on Computers, 2017, 66, 1435-1441.	2.4	201
2	A First Step Toward Cost Functions for Quantum-Dot Cellular Automata Designs. IEEE Nanotechnology Magazine, 2014, 13, 476-487.	1.1	161
3	A Retrospective and Prospective View of Approximate Computing [Point of View}. Proceedings of the IEEE, 2020, 108, 394-399.	16.4	114
4	Design and Evaluation of Approximate Logarithmic Multipliers for Low Power Error-Tolerant Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 2856-2868.	3.5	106
5	Machine Learning Security: Threats, Countermeasures, and Evaluations. IEEE Access, 2020, 8, 74720-74742.	2.6	94
6	Optimized Schoolbook Polynomial Multiplication for Compact Lattice-Based Cryptography on FPGA. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2459-2463.	2.1	70
7	Design and Analysis of Approximate Redundant Binary Multipliers. IEEE Transactions on Computers, 2019, 68, 804-819.	2.4	63
8	QCA Systolic Array Design. IEEE Transactions on Computers, 2013, 62, 548-560.	2.4	53
9	On the Design of Approximate Restoring Dividers for Error-Tolerant Applications. IEEE Transactions on Computers, 2016, 65, 2522-2533.	2.4	51
10	Approximate Designs for Fast Fourier Transform (FFT) With Application to Speech Recognition. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4727-4739.	3.5	49
11	Design of Approximate Unsigned Integer Non-restoring Divider for Inexact Computing. , 2015, , .		48
12	High Performance CNN Accelerators Based on Hardware and Algorithm Co-Optimization. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 250-263.	3.5	48
13	Hybrid Low Radix Encoding-Based Approximate Booth Multipliers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3367-3371.	2.2	45
14	Design and Analysis of Inexact Floating-Point Adders. IEEE Transactions on Computers, 2016, 65, 308-314.	2.4	44
15	Design and Analysis of Majority Logic-Based Approximate Adders and Multipliers. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 1609-1624.	3.2	44
16	A machine learning attack resistant multi-PUF design on FPGA. , 2018, , .		39
17	XOR-Based Low-Cost Reconfigurable PUFs for IoT Security. Transactions on Embedded Computing Systems, 2019, 18, 1-21.	2.1	37
18	A Modified Partial Product Generator for Redundant Binary Multipliers. IEEE Transactions on Computers, 2016, 65, 1165-1171.	2.4	36

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19	A Flip-Flop Based Arbiter Physical Unclonable Function (APUF) Design with High Entropy and Uniqueness for FPGA Implementation. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 1853-1866.	3.2	35
20	A Modeling Attack Resistant Deception Technique for Securing Lightweight-PUF-Based Authentication. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1183-1196.	1.9	34
21	An Efficient and Parallel R-LWE Cryptoprocessor. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 886-890.	2.2	33
22	Data Compression Device Based on Modified LZ4 Algorithm. IEEE Transactions on Consumer Electronics, 2018, 64, 110-117.	3.0	32
23	Ten years of hardware Trojans: a survey from the attacker's perspective. IET Computers and Digital Techniques, 2020, 14, 231-246.	0.9	32
24	XOR gate based low-cost configurable RO PUF. , 2017, , .		31
25	Design and Implementation of an Approximate Softmax Layer for Deep Neural Networks. , 2020, , .		31
26	Design and Analysis of Energy-Efficient Dynamic Range Approximate Logarithmic Multipliers for Machine Learning. IEEE Transactions on Sustainable Computing, 2021, 6, 612-625.	2.2	30
27	Algorithm and Design of a Fully Parallel Approximate Coordinate Rotation Digital Computer (CORDIC). IEEE Transactions on Multi-Scale Computing Systems, 2017, 3, 139-151.	2.5	29
28	One-to-N & N-to-One: Two Advanced Backdoor Attacks Against Deep Learning Models. IEEE Transactions on Dependable and Secure Computing, 2022, 19, 1562-1578.	3.7	29
29	Security in Approximate Computing and Approximate Computing for Security: Challenges and Opportunities. Proceedings of the IEEE, 2020, 108, 2214-2231.	16.4	28
30	Design of Majority Logic (ML) Based Approximate Full Adders. , 2018, , .		27
31	Ultra-Lightweight and Reconfigurable Tristate Inverter Based Physical Unclonable Function Design. IEEE Access, 2018, 6, 28478-28487.	2.6	25
32	Defeating Untrustworthy Testing Parties: A Novel Hybrid Clustering Ensemble Based Golden Models-Free Hardware Trojan Detection Method. IEEE Access, 2019, 7, 5124-5140.	2.6	25
33	AxBMs: Approximate Radix-8 Booth Multipliers for High-Performance FPGA-Based Accelerators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1566-1570.	2.2	25
34	Design, Evaluation and Application of Approximate High-Radix Dividers. IEEE Transactions on Multi-Scale Computing Systems, 2018, 4, 299-312.	2.5	24
35	Ultra High-Speed Polynomial Multiplications for Lattice-Based Cryptography on FPGAs. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 1993-2005.	3.2	24
36	A Real-Time Hardware Emulator for 3D Non-Stationary U2V Channels. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 3951-3964.	3.5	23

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37	Precision Adaptive MFCC Based on R2SDF-FFT and Approximate Computing for Low-Power Speech Keywords Recognition. IEEE Circuits and Systems Magazine, 2021, 21, 24-39.	2.6	23
38	Lattice-based Cryptography for IoT in A Quantum World: Are We Ready?. , 2019, , .		22
39	Resource-Shared Crypto-Coprocessor of AES Enc/Dec With SHA-3. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4869-4882.	3.5	21
40	QCA Systolic Matrix Multiplier. , 2010, , .		19
41	High-performance approximate half and full adder cells using NAND logic gate. IEICE Electronics Express, 2019, 16, 20190043-20190043.	0.3	19
42	Approximate Computing: From Circuits to Applications. Proceedings of the IEEE, 2020, 108, 2103-2107.	16.4	19
43	Hybrid Partial Product-Based High-Performance Approximate Recursive Multipliers. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 507-513.	3.2	19
44	Design and Performance Evaluation of Approximate Floating-Point Multipliers. , 2016, , .		18
45	Design of High-Speed Wide-Word Hybrid Parallel-Prefix/Carry-Select and Skip Adders. Journal of Signal Processing Systems, 2018, 90, 409-419.	1.4	18
46	Optimized Modular Multiplication for Supersingular Isogeny Diffie-Hellman. IEEE Transactions on Computers, 2019, 68, 1249-1255.	2.4	18
47	A Modeling Attack Resistant Deception Technique for Securing PUF based Authentication. , 2019, , .		18
48	Mathematical Modeling Analysis of Strong Physical Unclonable Functions. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4426-4438.	1.9	18
49	Design of Majority Logic-Based Approximate Booth Multipliers for Error-Tolerant Applications. IEEE Nanotechnology Magazine, 2022, 21, 81-89.	1.1	18
50	Combining Restoring Array and Logarithmic Dividers into an Approximate Hybrid Design. , 2018, , .		17
51	Design of Approximate High-Radix Dividers by Inexact Binary Signed-Digit Addition. , 2017, , .		16
52	A Highly Flexible Lightweight and High Speed True Random Number Generator on FPGA. , 2018, , .		16
53	New Majority Gate-Based Parallel BCD Adder Designs for Quantum-Dot Cellular Automata. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1232-1236.	2.2	16
54	Lightweight Modeling Attack-Resistant Multiplexer-Based Multi-PUF (MMPUF) Design on FPGA. Electronics (Switzerland), 2020, 9, 815.	1.8	16

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55	High Performance Parallel Decimal Multipliers Using Hybrid BCD Codes. IEEE Transactions on Computers, 2017, 66, 1994-2004.	2.4	15
56	Designs of Approximate Floating-Point Multipliers with Variable Accuracy for Error-Tolerant Applications. Journal of Signal Processing Systems, 2018, 90, 641-654.	1.4	15
57	A Theoretical Model to Link Uniqueness and Min-Entropy for PUF Evaluations. IEEE Transactions on Computers, 2019, 68, 287-293.	2.4	15
58	High Performance Modular Multiplication for SIDH. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3118-3122.	1.9	15
59	Lightweight Hardware Implementation of R-LWE Lattice-Based Cryptography. , 2018, , .		14
60	A Novel Feature Extraction Strategy for Hardware Trojan Detection. , 2020, , .		14
61	Background Calibration of Bit Weights in Pipelined-SAR ADCs Using Paired Comparators. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1074-1078.	2.1	14
62	A large-scale comprehensive evaluation of single-slice ring oscillator and PicoPUF bit cells on 28-nm Xilinx FPGAs. Journal of Cryptographic Engineering, 2021, 11, 227-238.	1.5	14
63	Intellectual Property Protection for Deep Learning Models: Taxonomy, Methods, Attacks, and Evaluations. IEEE Transactions on Artificial Intelligence, 2022, 3, 908-923.	3.4	14
64	More is Less: Domain-Specific Speech Recognition Microprocessor Using One-Dimensional Convolutional Recurrent Neural Network. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 1571-1582.	3.5	13
65	Inexact floating-point adder for dynamic image processing. , 2014, , .		12
66	Design of Approximate Logarithmic Multipliers. , 2017, , .		12
67	Cost-efficient decimal adder design in Quantum-dot cellular automata. , 2012, , .		11
68	AxMM: Area and Power Efficient Approximate Modular Multiplier for R-LWE Cryptosystem. , 2020, , .		11
69	Backdoors hidden in facial features: a novel invisible backdoor attack against face recognition systems. Peer-to-Peer Networking and Applications, 2021, 14, 1458-1474.	2.6	11
70	Building an accurate hardware Trojan detection technique from inaccurate simulation models and unlabelled ICs. IET Computers and Digital Techniques, 2019, 13, 348-359.	0.9	10
71	DC-LSTM: Deep Compressed LSTM with Low Bit-Width and Structured Matrices. , 2020, , .		10
72	BCD Adder Designs Based on Three-Input XOR and Majority Gates. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1942-1946.	2.2	10

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73	Stochastic Dividers for Low Latency Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4102-4115.	3.5	10
74	Transformer PUF : A Highly Flexible Configurable RO PUF Based on FPGA. , 2020, , .		9
75	Profile-Based Output Error Compensation for Approximate Arithmetic Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4707-4718.	3.5	9
76	A Physical Unclonable Function Using a Configurable Tristate Hybrid Scheme With Non-Volatile Memory. IEEE Open Journal of Nanotechnology, 2021, 2, 31-40.	0.9	9
77	A Dynamically Configurable PUF and Dynamic Matching Authentication Protocol. IEEE Transactions on Emerging Topics in Computing, 2021, , 1-1.	3.2	9
78	Design of An Approximate FFT Processor Based on Approximate Complex Multipliers. , 2021, , .		9
79	Security Analysis of Hardware Trojans on Approximate Circuits. , 2020, , .		9
80	PTB: Robust physical backdoor attacks against deep neural networks in real world. Computers and Security, 2022, 118, 102726.	4.0	9
81	A Parallel Decimal Multiplier Using Hybrid Binary Coded Decimal (BCD) Codes. , 2016, , .		8
82	Design and Optimization of Modular Multiplication for SIDH. , 2018, , .		8
83	Design and Analysis of Majority Logic Based Approximate Radix-4 Booth Encoders. , 2019, , .		8
84	Active DNN IP Protection: A Novel User Fingerprint Management and DNN Authorization Control Technique. , 2020, , .		8
85	A High-Performance SIKE Hardware Accelerator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 803-815.	2.1	8
86	Montgomery modular multiplier design in quantum-dot cellular automata using cut-set retiming. , 2010, , .		7
87	Approximate Computing and Its Application to Hardware Security. , 2018, , 43-67.		7
88	A Co-training Based Hardware Trojan Detection Technique by Exploiting Unlabeled ICs and Inaccurate Simulation Models. , 2018, , .		7
89	Theoretical Analysis of Delay-Based PUFs and Design Strategies for Improvement. , 2019, , .		7
90	Design of Unsigned Approximate Hybrid Dividers Based on Restoring Array and Logarithmic Dividers. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 339-350.	3.2	7

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91	Lightweight Configurable Ring Oscillator PUF Based on RRAM/CMOS Hybrid Circuits. IEEE Open Journal of Nanotechnology, 2020, 1, 128-134.	0.9	7
92	Towards CRYSTALS-Kyber: A M-LWE Cryptoprocessor with Area-Time Trade-Off. , 2021, , .		7
93	AxRLWE: A Multilevel Approximate Ring-LWE Co-Processor for Lightweight IoT Applications. IEEE Internet of Things Journal, 2022, 9, 10492-10501.	5.5	7
94	Robust Backdoor Attacks against Deep Neural Networks in Real Physical World. , 2021, , .		7
95	Design of Approximate FFT with Bit-width Selection Algorithms. , 2018, , .		6
96	A Hardware/Software Co-design Method for Approximate Semi-Supervised K-Means Clustering. , 2018, , .		6
97	Reduced Precision Redundancy for Reliable Processing of Data. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 1960-1971.	3.2	6
98	Design and Evaluation of a Power-Efficient Approximate Systolic Array Architecture for Matrix Multiplication. , 2019, , .		6
99	INA: Incremental Network Approximation Algorithm for Limited Precision Deep Neural Networks. , 2019, , .		6
100	AxSA: On the Design of High-Performance and Power-Efficient Approximate Systolic Arrays for Matrix Multiplication. Journal of Signal Processing Systems, 2021, 93, 605-615.	1.4	6
101	A Hardware/Software Co-Design Methodology for Adaptive Approximate Computing in clustering and ANN Learning. IEEE Open Journal of the Computer Society, 2021, 2, 38-52.	5.2	6
102	A lightweight key renewal scheme based authentication protocol with configurable RO PUF for clustered sensor networks. Microelectronics Journal, 2021, 117, 105265.	1.1	6
103	GBC: An Energy-Efficient LSTM Accelerator With Gating Units Level Balanced Compression Strategy. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 3655-3665.	3.5	6
104	APAS: Application-Specific Accelerators for RLWE-Based Homomorphic Linear Transformations. IEEE Transactions on Information Forensics and Security, 2021, 16, 4663-4678.	4.5	5
105	A Generic Dynamic Responding Mechanism and Secure Authentication Protocol for Strong PUFs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1256-1268.	2.1	5
106	A review of QCA adders and metrics. , 2012, , .		4
107	A Reconfigurable Memory PUF Based on Tristate Inverter Arrays. , 2016, , .		4
108	DC MUX PUF: A highly reliable feed-back MUX PUF based on measuring duty cycle. , 2017, , .		4

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109	Design of Dynamic Range Approximate Logarithmic Multipliers. , 2018, , .		4
110	DPAEG: A Dependency Parse-Based Adversarial Examples Generation Method for Intelligent Q&A Robots. Security and Communication Networks, 2020, 2020, 1-15.	1.0	4
111	Background Calibration for Bit Weights in Pipelined ADCs Using Adaptive Dither Windows. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1783-1787.	2.2	4
112	GOMIL: Global Optimization of Multiplier by Integer Linear Programming. , 2021, , .		4
113	High-Performance Systolic Array Montgomery Multiplier for SIKE. , 2021, , .		4
114	An Energy Efficient Accelerator for Bidirectional Recurrent Neural Networks (BiRNNs) Using Hybrid-Iterative Compression With Error Sensitivity. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 3707-3718.	3.5	4
115	Active intellectual property protection for deep neural networks through stealthy backdoor and usersâ€™ identities authentication. Applied Intelligence, 2022, 52, 16497-16511.	3.3	4
116	A High-Speed CNN Hardware Accelerator with Regular Pruning. , 2022, , .		4
117	Multiprecision Multiplication on ARMv8. , 2017, , .		3
118	Theoretical Analysis of Configurable RO PUFs and Strategies to Enhance Security. , 2019, , .		3
119	A Dynamic Highly Reliable SRAM-Based PUF Retaining Memory Function. , 2021, , .		3
120	A 10-b 500MS/s Partially Loop-Unrolled SAR ADC with a Comparator Offset Calibration Technique. , 2021, , .		3
121	Design, evaluation and application of approximateâ€truncated Booth multipliers. IET Circuits, Devices and Systems, 2020, 14, 1305-1317.	0.9	3
122	PAxC: A Probabilistic-oriented Approximate Computing Methodology for ANNs. , 2022, , .		3
123	Data Stream Oriented Fine-grained Sparse CNN Accelerator with Efficient Unstructured Pruning Strategy. , 2022, , .		3
124	Design of 3-D quantum-dot cellular automata adders. IEICE Electronics Express, 2015, 12, 20150195-20150195.	0.3	2
125	Multi-Incentive Delay-Based (MID) PUF. , 2019, , .		2
126	Guest Editorial: Introduction to the Special Section on Cyber Security Threats and Defense Advance. IEEE Transactions on Emerging Topics in Computing, 2020, 8, 264-266.	3.2	2

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127	An Efficient High SFDR PDDS Using High-Pass-Shaped Phase Dithering. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 2003-2007.	2.1	2
128	Detect and Remove Watermark in Deep Neural Networks via Generative Adversarial Networks. Lecture Notes in Computer Science, 2021, , 341-357.	1.0	2
129	Low-Power Approximate RPR Scheme for Unsigned Integer Arithmetic Computation. IEEE Open Journal of Nanotechnology, 2022, 3, 36-44.	0.9	2
130	A survey of approximate arithmetic circuits and blocks. IT - Information Technology, 2022, 64, 79-87.	0.6	2
131	Design and analysis of hardware Trojans in approximate circuits. Electronics Letters, 2022, 58, 197-199.	0.5	2
132	Bit erasure analysis of binary adders in Quantum-dot Cellular Automata. , 2014, , .		1
133	Notice of Violation of IEEE Publication Principles: Application of LDPC codes on PUF error correction based on code-offset construction. , 2017, , .		1
134	A 2-Then-1 Bit/Cycle Asynchronous SAR ADC with Background Offset Calibration. , 2021, , .		1
135	Live demonstration: An automatic evaluation platform for physical unclonable function test. , 2016, , .		1
136	An Efficient Hardware Generator for Massive Non-Stationary Fading Channels. , 2020, , .		1
137	Design and analysis of energyâ€efficient approximate Boothâ€folding squarers with precision recovery. Electronics Letters, 2022, 58, 349-351.	0.5	1
138	Dynamically Configurable Physical Unclonable Function based on RRAM Crossbar. , 2021, , .		1
139	Use the Spear as a Shield: An Adversarial Example Based Privacy-Preserving Technique Against Membership Inference Attacks. IEEE Transactions on Emerging Topics in Computing, 2023, 11, 153-169.	3.2	1
140	A High Performance SIKE Accelerator With High Frequency and Low Area-Time Product. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3899-3903.	2.2	1
141	Dataset authorization control: protect the intellectual property of dataset via reversible feature space adversarial examples. Applied Intelligence, 2023, 53, 7298-7309.	3.3	1
142	Security Analysis and Modeling Attacks on Duty Cycle Multiplexer PUF. , 2019, , .		0
143	Dynamic Reconfigurable PUFs Based on FPGA. , 2019, , .		0
144	Security and Approximation: Vulnerabilities in Approximation-Aware Testing. IEEE Transactions on Emerging Topics in Computing, 2023, 11, 265-271.	3.2	0

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145	An Energy-efficient and High-precision Approximate MAC with Distributed Arithmetic Circuits. , 2022, , .		0
146	Editorial Special Issue on Circuits and Systems for Emerging Computing Paradigms. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 2653-2654.	3.5	0