Xiaoyu Sun

List of Publications by Year
in descending order

22 papers	1,003 citations	759233 12 h-index	1199594 12 g-index
22 all docs	22 docs citations	22 times ranked	855 citing authors

#	Article	IF	Citations
1	DNN+NeuroSim: An End-to-End Benchmarking Framework for Compute-in-Memory Accelerators with Versatile Device Technologies. , 2019, , .		154
2	XNOR-RRAM: A scalable and parallel resistive synaptic architecture for binary neural networks. , 2018, , .		133
3	A Twin-8T SRAM Computation-in-Memory Unit-Macro for Multibit CNN-Based AI Edge Processors. IEEE Journal of Solid-State Circuits, 2020, 55, 189-202.	5.4	108
4	Impact of Non-Ideal Characteristics of Resistive Synaptic Devices on Implementing Convolutional Neural Networks. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 570-579.	3.6	100
5	A Dual-Split 6T SRAM-Based Computing-in-Memory Unit-Macro With Fully Parallel Product-Sum Operation for Binarized DNN Edge Processors. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4172-4185.	5.4	93
6	High-Throughput In-Memory Computing for Binary Deep Neural Networks With Monolithically Integrated RRAM and 90-nm CMOS. IEEE Transactions on Electron Devices, 2020, 67, 4185-4192.	3.0	92
7	Exploiting Hybrid Precision for Training and Inference: A 2T-1FeFET Based Analog Synaptic Weight Cell. , 2018, , .		71
8	Characterizing Endurance Degradation of Incremental Switching in Analog RRAM for Neuromorphic Systems. , 2018, , .		44
9	2-Bit-Per-Cell RRAM-Based In-Memory Computing for Area-/Energy-Efficient Deep Learning. IEEE Solid-State Circuits Letters, 2020, 3, 194-197.	2.0	39
10	A Highly Reliable RRAM Physically Unclonable Function Utilizing Post-Process Randomness Source. IEEE Journal of Solid-State Circuits, 2021, 56, 1641-1650.	5.4	32
11	A 40-nm MLC-RRAM Compute-in-Memory Macro With Sparsity Control, On-Chip Write-Verify, and Temperature-Independent ADC References. IEEE Journal of Solid-State Circuits, 2022, 57, 2868-2877.	5.4	21
12	Benchmark of Ferroelectric Transistor-Based Hybrid Precision Synapse for Neural Network Accelerator. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2019, 5, 142-150.	1.5	20
13	Low-VDD Operation of SRAM Synaptic Array for Implementing Ternary Neural Network. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2962-2965.	3.1	19
14	Investigating Ferroelectric Minor Loop Dynamics and History Effectâ€"Part I: Device Characterization. IEEE Transactions on Electron Devices, 2020, 67, 3592-3597.	3.0	18
15	Heterogeneous Mixed-Signal Monolithic 3-D In-Memory Computing Using Resistive RAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 386-396.	3.1	18
16	Investigating Ferroelectric Minor Loop Dynamics and History Effectâ€"Part II: Physical Modeling and Impact on Neural Network Training. IEEE Transactions on Electron Devices, 2020, 67, 3598-3604.	3.0	15
17	Overcoming Challenges for Achieving High in-situ Training Accuracy with Emerging Memories. , 2020, , .		8
18	A Parallel RRAM Synaptic Array Architecture for Energy-Efficient Recurrent Neural Networks. , 2018, , .		6

#	Article	IF	Citations
19	A Versatile ReRAM-based Accelerator for Convolutional Neural Networks. , 2018, , .		6
20	Characterization and Mitigation of Relaxation Effects on Multi-level RRAM based In-Memory Computing. , 2021, , .		6
21	A 40nm RRAM Compute-in-Memory Macro Featuring On-Chip Write-Verify and Offset-Cancelling ADC References. , 2021, , .		0
22	Achieving High In Situ Training Accuracy and Energy Efficiency with Analog Non-Volatile Synaptic Devices. ACM Transactions on Design Automation of Electronic Systems, 2022, 27, 1-19.	2.6	0