Mario Donato Marino

List of Publications by Year
in descending order

28 papers	144 citations	1684188 5 h-index	1720034 7 g-index
29 all docs	29 docs citations	29 times ranked	62 citing authors

#	Article	IF	Citations
1	An Evolutionary-Based Approach for Low-Complexity Intrusion Detection in Wireless Sensor Networks. Wireless Personal Communications, 2022, 126, 2019-2042.	2.7	6
2	A novel secure DV-Hop localization algorithm against wormhole attacks. Telecommunication Systems, 2022, 80, 413-430.	2.5	3
3	Walter: Wide I/O Scaling of Number of Memory Controllers Versus Frequency and Voltage. IEEE Access, 2020, 8, 193874-193889.	4.2	1
4	On parallelisation of image dehazing with OpenMP. International Journal of Embedded Systems, 2019, 11, 427.	0.3	2
5	RAMON: Region-Aware Memory Controller. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 697-710.	3.1	4
6	Exploiting dynamic transaction queue size in scalable memory systems. Soft Computing, 2018, 22, 2065-2077.	3.6	2
7	An efficient algorithm for modelling and dynamic prediction of network traffic. International Journal of Computational Science and Engineering, 2018, 16, 311.	0.5	6
8	Architectural Impacts of RFiop: RF to Address I/O Pad and Memory Controller Scalability. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1494-1507.	3.1	2
9	System implications of LLC MSHRs in scalable memory systems. Microprocessors and Microsystems, 2017, 52, 355-364.	2.8	5
10	ABaT-FS: Towards adjustable bandwidth and temperature via frequency scaling in scalable memory systems. Microprocessors and Microsystems, 2016, 45, 339-354.	2.8	3
11	Implications of shallower memory controller transaction queues in scalable memory systems. Journal of Supercomputing, 2016, 72, 1785-1798.	3.6	5
12	Last level cache size heterogeneity in embedded systems. Journal of Supercomputing, 2016, 72, 503-544.	3.6	6
13	GPU Computations on Hadoop Clusters for Massive Data Processing. Lecture Notes in Electrical Engineering, 2016, , 515-521.	0.4	0
14	Insights on memory controller scaling in multi-core embedded systems. International Journal of Embedded Systems, 2014, 6, 351.	0.3	10
15	RFiof. , 2013, , .		6
16	On-Package Scalability of RF and Inductive Memory Controllers. , 2012, , .		7
17	RFiop: RF-memory path to address on-package I/O pad and memory controller scalability. , 2012, , .		9
18	Adapted discrete-based entropy cache replacement algorithm. , 2012, , .		1

#	Article	IF	Citations
19	An evaluation of the TRIPS computer system. ACM SIGPLAN Notices, 2009, 44, 1-12.	0.2	7
20	An evaluation of the TRIPS computer system. , 2009, , .		48
21	An evaluation of the TRIPS computer system. Computer Architecture News, 2009, 37, 1-12.	2.5	3
22	32-core CMP with multi-sliced L2: 2 and 4 cores sharing a L2 slice. , 2006, , .		4
23	L2-Cache Hierarchical Organizations for Multi-core Architectures. Lecture Notes in Computer Science, 2006, , 74-83.	1.3	3
24	A Preliminary Study of Cache-Only Write Detection Technique for Nautilus DSM. Kluwer International Series in Engineering and Computer Science, 2002, , 275-289.	0.2	0
25	A Preliminary DSM Speedup Comparison: JIAJIA X Nautilus. , 2002, , 413-428.		1
26	Influence of the dynamic page aggregation on the speedup of Nautilus DSM system. , 0, , .		0
27	A speedup comparative study: three third generation DSM systems. , 0, , .		0
28	Evaluating the speedup of a MPI-based distributed dispersion simulator for groundwater systems. , 0, , .		0