Xiaoqing Wen

List of Publications by Year
in descending order

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59	882	471061	580395
papers	citations	17	25
		h-index	g-index

59	59	59	341
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Novel Low Cost, Double-and-Triple-Node-Upset-Tolerant Latch Designs for Nano-scale CMOS. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 520-533.	3.2	68
2	Information Assurance Through Redundant Design: A Novel TNU Error-Resilient Latch for Harsh Radiation Environment. IEEE Transactions on Computers, 2020, 69, 789-799.	2.4	66
3	LCHR-TSV: Novel Low Cost and Highly Repairable Honeycomb-Based TSV Redundancy Architecture for Clustered Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2938-2951.	1.9	55
4	Design of a Triple-Node-Upset Self-Recoverable Latch for Aerospace Applications in Harsh Radiation Environments. IEEE Transactions on Aerospace and Electronic Systems, 2020, 56, 1163-1171.	2.6	52
5	Novel Speed-and-Power-Optimized SRAM Cell Designs With Enhanced Self-Recoverability From Single- and Double-Node Upsets. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4684-4695.	3.5	50
6	Novel Quadruple-Node-Upset-Tolerant Latch Designs With Optimized Overhead for Reliable Computing in Harsh Radiation Environments. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 404-413.	3.2	49
7	Non-Intrusive Online Distributed Pulse Shrinking-Based Interconnect Testing in 2.5D IC. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2657-2661.	2.2	40
8	A Novel TDMA-Based Fault Tolerance Technique for the TSVs in 3D-ICs Using Honeycomb Topology. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 724-734.	3.2	39
9	Novel Double-Node-Upset-Tolerant Memory Cell Designs Through Radiation-Hardening-by-Design and Layout. IEEE Transactions on Reliability, 2019, 68, 354-363.	3.5	37
10	A Secure and Multiobjective Virtual Machine Placement Framework for Cloud Data Center. IEEE Systems Journal, 2022, 16, 3163-3174.	2.9	36
11	Quadruple and Sextuple Cross-Coupled SRAM Cell Designs With Optimized Overhead for Reliable Applications. IEEE Transactions on Device and Materials Reliability, 2022, 22, 282-295.	1.5	34
12	Quadruple Cross-Coupled Dual-Interlocked-Storage-Cells-Based Multiple-Node-Upset-Tolerant Latch Designs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 879-890.	3.5	32
13	A Double-Node-Upset Self-Recoverable Latch Design for High Performance and Low Power Application. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 287-291.	2.2	29
14	A Cost-Effective TSV Repair Architecture for Clustered Faults in 3-D IC. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1952-1956.	1.9	29
15	A Novel Low-Cost TMR-Without-Voter Based HIS-Insensitive and MNU-Tolerant Latch Design for Aerospace Applications. IEEE Transactions on Aerospace and Electronic Systems, 2020, 56, 2666-2676.	2.6	24
16	Reducing Power Supply Noise in Linear-Decompressor-Based Test Data Compression Environment for At-Speed Scan Testing. , 2008, , .		22
17	Novel Quadruple Cross-Coupled Memory Cell Designs With Protection Against Single Event Upsets and Double-Node Upsets. IEEE Access, 2019, 7, 176188-176196.	2.6	20
18	Cost-Effective and Highly Reliable Circuit-Components Design for Safety-Critical Applications. IEEE Transactions on Aerospace and Electronic Systems, 2022, 58, 517-529.	2.6	20

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19	A Novel and Practical Control Scheme for Inter-Clock At-Speed Testing. IEEE International Test Conference (TC), 2006, , .	0.0	17
20	Power Supply Noise Reduction for At-Speed Scan Testing in Linear-Decompression Environment. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1767-1776.	1.9	15
21	A Novel Triple-Node-Upset-Tolerant CMOS Latch Design using Single-Node-Upset-Resilient Cells. , 2019, , .		13
22	On test pattern compaction with multi-cycle and multi-observation scan test. , 2010, , .		10
23	A Transition Isolation Scan Cell Design for Low Shift and Capture Power. , 2012, , .		10
24	Single-Event Double-Upset Self-Recoverable and Single-Event Transient Pulse Filterable Latch Design for Low Power Applications. , 2019, , .		10
25	Dual-modular-redundancy and dual-level error-interception based triple-node-upset tolerant latch designs for safety-critical applications. Microelectronics Journal, 2021, 111, 105034.	1.1	8
26	Turbo1500: Toward Core-Based Design for Test and Diagnosis Using the IEEE 1500 Standard. , 2008, , .		7
27	Fault Detection with Optimum March Test Algorithm. , 2012, , .		7
28	TPDICE and Sim Based 4-Node-Upset Completely Hardened Latch Design for Highly Robust Computing in Harsh Radiation. , 2021, , .		7
29	Ultrascan: using time-division demultiplexing/multiplexing (TDDM/TDM) with virtualscan for test cost reduction. , 0, , .		6
30	Design of a Highly Reliable SRAM Cell with Advanced Self-Recoverability from Soft Errors. , 2020, , .		6
31	Diagnosis of Realistic Defects Based on the X-Fault Model. , 2008, , .		5
32	A 4NU-Recoverable and HIS-Insensitive Latch Design for Highly Robust Computing in Harsh Radiation Environments. , 2021, , .		5
33	Designs of Level-Sensitive T Flip-Flops and Polar Encoders Based on Two XOR/XNOR Gates. Electronics (Switzerland), 2022, 11, 1658.	1.8	5
34	On Improving Defect Coverage of Stuck-at Fault Tests. , 2005, , .		4
35	Design of a Sextuple Cross-Coupled SRAM Cell with Optimized Access Operations for Highly Reliable Terrestrial Applications. , 2019, , .		4
36	Dual-Interlocked-Storage-Cell-Based Double-Node-Upset Self-Recoverable Flip-Flop Design for Safety-Critical Applications. , 2020, , .		4

#	Article	IF	Citations
37	Design of Radiation Hardened Latch and Flip-Flop with Cost-Effectiveness for Low-Orbit Aerospace Applications. Journal of Electronic Testing: Theory and Applications (JETTA), 0, , 1.	0.9	4
38	A double-node-upset completely tolerant CMOS latch design with extremely low cost for high-performance applications. The Integration VLSI Journal, 2022, 86, 22-29.	1.3	4
39	Clock-gating-aware low launch WSA test pattern generation for at-speed scan testing. , 2011, , .		3
40	HITTSFL: Design of a Cost-Effective HIS-Insensitive TNU-Tolerant and SET-Filterable Latch for Safety-Critical Applications. , 2020, , .		3
41	A Sextuple Cross-Coupled SRAM Cell Protected against Double-Node Upsets. , 2020, , .		3
42	A Sextuple Cross-Coupled Dual-Interlocked-Storage-Cell based Multiple-Node-Upset Self-Recoverable Latch. , 2021, , .		3
43	SCLCRL: Shuttling C-elements based Low-Cost and Robust Latch Design Protected against Triple Node Upsets in Harsh Radiation Environments. , 2022, , .		3
44	Broadcast-TDMA: A Cost-Effective Fault-Tolerance Method for TSV Lifetime Reliability Enhancement. IEEE Design and Test, 2022, 39, 34-42.	1.1	3
45	Hybrid fault simulation with compiled and event-driven methods. , 2006, , .		2
46	Testing Static Single Cell Faults using static and dynamic data background. , 2011, , .		2
47	Practical Challenges in Logic BIST Implementation – Case Studies. , 2008, , .		1
48	Reseeding-Oriented Test Power Reduction for Linear-Decompression-Based Test Compression Architectures. IEICE Transactions on Information and Systems, 2016, E99.D, 2672-2681.	0.4	1
49	Novel Radiation Hardened Latch Design with Cost-Effectiveness for Safety-Critical Terrestrial Applications. , 2019, , .		1
50	A Reliable and Low-Cost Flip-Flop Hardened against Double-Node-Upsets. , 2021, , .		1
51	Evaluation and Test of Production Defects in Hardened Latches. IEICE Transactions on Information and Systems, 2022, E105.D, 996-1009.	0.4	1
52	A Highly Robust, Low Delay and DNU-Recovery Latch Design for Nanoscale CMOS Technology. , 2022, , .		1
53	A Highly Reliable and Low Power RHBD Flip-Flop Cell for Aerospace Applications. , 2022, , .		1
54	On Optimizing Fault Coverage, Pattern Count, and ATPG Run Time Using a Hybrid Single-Capture Scheme for Testing Scan Designs. , 2008, , .		0

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55	Case Studies on Transition Fault Test Generation for At-speed Scan Testing. , 2010, , .		0
56	Cellular Structure-Based Fault-Tolerance TSV Configuration in 3D-IC. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1196-1208.	1.9	0
57	Fortune: A New Fault-Tolerance TSV Configuration in Router-Based Redundancy Structure. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3182-3187.	1.9	0
58	Two 0.8 V, Highly Reliable RHBD 10T and 12T SRAM Cells for Aerospace Applications. , 2022, , .		0
59	Sextuple Cross-Coupled-DICE Based Double-Node-Upset Recoverable and Low-Delay Flip-Flop for Aerospace Applications. , 2022, , .		0