Ramon Bertran Monfort

List of Publications by Year
in descending order

31	537	1684188 5	1474206 9
papers	citations	h-index	g-index

31	31	31	429
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	AI accelerator on IBM Telum processor. , 2022, , .		3
2	Intelligent Adaptation of Hardware Knobs for Improving Performance and Power Consumption. IEEE Transactions on Computers, 2021, 70, 1-16.	3.4	3
3	Predictive Guardbanding: Program-Driven Timing Margin Reduction for GPUs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 171-184.	2.7	5
4	Cores, Cache, Content, and Characterization: IBMâ€™s Second Generation 14-nm Product, z15. IEEE Journal of Solid-State Circuits, 2021, 56, 98-111.	5.4	4
5	MicroGrad: A Centralized Framework for Workload Cloning and Stress Testing. , 2021, , .		2
6	Energy Efficiency Boost in the AI-Infused POWER10 Processor. , 2021, , .		8
7	SERMiner : A Framework for Early-stage Reliability Estimation for IBM Processors. , 2021, , .		2
8	2.7 IBM z15: A 12-Core 5.2GHz Microprocessor. , 2020, , .		13
9	Asymmetric Resilience: Exploiting Task-Level Idempotency for Transient Error Recovery in Accelerator-Based Systems. , 2020, , .		14
10	Generation of Stressmarks for Early Stage Soft-Error Modeling. , 2019, , .		1
11	Asymmetric Resilience for Accelerator-Rich Systems. IEEE Computer Architecture Letters, 2019, 18, 83-86.	1.5	2
12	IBM z14: Processor Characterization and Power Management for High-Reliability Mainframe Systems. IEEE Journal of Solid-State Circuits, 2019, 54, 121-132.	5.4	11
13	Droop mitigation using critical-path sensors and an on-chip distributed power supply estimation engine in the z14â„¢ enterprise processor. , 2018, , .		16
14	ChopStiX: Systematic Extraction of Code-Representative Microbenchmarks. , 2018, , .		4
15	26.2 Power supply noise in a 22nm z13â„¢ microprocessor. , 2017, , .		13
16	BRAVO: Balanced Reliability-Aware Voltage Optimization. , 2017, , .		24
17	libPRISM. , 2017, , .		2
18	Very Low Voltage (VLV) Design. , 2017, , .		5

#	Article	IF	Citations
19	Safe limits on voltage reduction efficiency in GPUs. , 2015, , .		60
20	Voltage Noise in Multi-Core Processors: Empirical Characterization and Optimization Opportunities. , 2014, , .		52
21	Characterization of transient error tolerance for a class of mobile embedded applications. , 2014, , .		2
22	A Systematic Methodology to Generate Decomposable and Responsive Power Models for CMPs. IEEE Transactions on Computers, 2013, 62, 1289-1302.	3.4	57
23	Counter-Based Power Modeling Methods: Top-Down vs. Bottom-Up. Computer Journal, 2013, 56, 198-213.	2.4	21
24	POTRA. , 2012, , .		2
25	POTRA. Performance Evaluation Review, 2012, 40, 427-428.	0.6	0
26	Systematic Energy Characterization of CMP/SMT Processor Systems via Automated Micro-Benchmarks. , 2012, , .		34
27	Energy accounting for shared virtualized environments under DVFS using PMC-based power models. Future Generation Computer Systems, 2012, 28, 457-468.	7.5	35
28	Design space exploration for aggressive core replication schemes in CMPs. , 2011, , .		0
29	Local Memory Design Space Exploration for High-Performance Computing. Computer Journal, 2011, 54, 786-799.	2.4	10
30	Accurate energy accounting for shared virtualized environments using PMC-based power modeling techniques. , 2010, , .		25
31	Decomposable and responsive power models for multicore processors using performance counters. , 2010, , .		107