

Zhengfeng Huang

List of Publications by Year in descending order

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56
papers

1,086
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430874

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all docs

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docs citations

58
times ranked

516
citing authors

| # | ARTICLE | IF | CITATIONS |
|----|--|-----|-----------|
| 1 | Architecture of Cobweb-Based Redundant TSV for Clustered Faults. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1736-1739. | 3.1 | 132 |
| 2 | Double-Node-Upset-Resilient Latch Design for Nanoscale CMOS Technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1978-1982. | 3.1 | 86 |
| 3 | Novel Low Cost, Double-and-Triple-Node-Upset-Tolerant Latch Designs for Nano-scale CMOS. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 520-533. | 4.6 | 68 |
| 4 | Information Assurance Through Redundant Design: A Novel TNU Error-Resilient Latch for Harsh Radiation Environment. IEEE Transactions on Computers, 2020, 69, 789-799. | 3.4 | 66 |
| 5 | A High Performance SEU Tolerant Latch. Journal of Electronic Testing: Theory and Applications (JETTA), 2015, 31, 349-359. | 1.2 | 57 |
| 6 | LCHR-TSV: Novel Low Cost and Highly Repairable Honeycomb-Based TSV Redundancy Architecture for Clustered Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2938-2951. | 2.7 | 55 |
| 7 | Novel Quadruple-Node-Upset-Tolerant Latch Designs With Optimized Overhead for Reliable Computing in Harsh Radiation Environments. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 404-413. | 4.6 | 49 |
| 8 | A Self-Recoverable, Frequency-Aware and Cost-Effective Robust Latch Design for Nanoscale CMOS Technology. IEICE Transactions on Electronics, 2015, E98.C, 1171-1178. | 0.6 | 41 |
| 9 | Non-Intrusive Online Distributed Pulse Shrinking-Based Interconnect Testing in 2.5D IC. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2657-2661. | 3.0 | 40 |
| 10 | A Novel TDMA-Based Fault Tolerance Technique for the TSVs in 3D-ICs Using Honeycomb Topology. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 724-734. | 4.6 | 39 |
| 11 | Quadruple and Sextuple Cross-Coupled SRAM Cell Designs With Optimized Overhead for Reliable Applications. IEEE Transactions on Device and Materials Reliability, 2022, 22, 282-295. | 2.0 | 34 |
| 12 | High-Throughput Portable True Random Number Generator Based on Jitter-Latch Structure. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 741-750. | 5.4 | 33 |
| 13 | Quadruple Cross-Coupled Dual-Interlocked-Storage-Cells-Based Multiple-Node-Upset-Tolerant Latch Designs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 879-890. | 5.4 | 32 |
| 14 | A Double-Node-Upset Self-Recoverable Latch Design for High Performance and Low Power Application. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 287-291. | 3.0 | 29 |
| 15 | A Cost-Effective TSV Repair Architecture for Clustered Faults in 3-D IC. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1952-1956. | 2.7 | 29 |
| 16 | High-performance, low-cost, and highly reliable radiation hardened latch design. Electronics Letters, 2016, 52, 139-141. | 1.0 | 24 |
| 17 | Design of a Radiation Hardened Latch for Low-Power Circuits. , 2014, , . | | 21 |
| 18 | Novel Quadruple Cross-Coupled Memory Cell Designs With Protection Against Single Event Upsets and Double-Node Upsets. IEEE Access, 2019, 7, 176188-176196. | 4.2 | 20 |

| # | ARTICLE | IF | CITATIONS |
|----|--|-----|-----------|
| 19 | Cost-Effective and Highly Reliable Circuit-Components Design for Safety-Critical Applications. IEEE Transactions on Aerospace and Electronic Systems, 2022, 58, 517-529. | 4.7 | 20 |
| 20 | Jitter-Quantizing-Based TRNG Robust Against PVT Variations. IEEE Access, 2020, 8, 108482-108490. | 4.2 | 18 |
| 21 | A Novel Triple-Node-Upset-Tolerant CMOS Latch Design using Single-Node-Upset-Resilient Cells. , 2019, , . | | 13 |
| 22 | A Region-Based Through-Silicon via Repair Method for Clustered Faults. IEICE Transactions on Electronics, 2017, E100.C, 1108-1117. | 0.6 | 13 |
| 23 | A highly reliable butterfly PUF in SRAM-based FPGAs. IEICE Electronics Express, 2017, 14, 20170551-20170551. | 0.8 | 11 |
| 24 | Rapid detection of trace Cu 2+ using an L-cysteine based interdigitated electrode sensor integrated with AC electrokinetic enrichment. Electrophoresis, 2019, 40, 2699-2705. | 2.4 | 11 |
| 25 | FPGA-based RO PUF with low overhead and high stability. Electronics Letters, 2019, 55, 510-513. | 1.0 | 10 |
| 26 | Pattern Reorder for Test Cost Reduction Through Improved SVMRANK Algorithm. IEEE Access, 2020, 8, 147965-147972. | 4.2 | 10 |
| 27 | Vernier ring based pre-bond through silicon vias test in 3D ICs. IEICE Electronics Express, 2017, 14, 20170590-20170590. | 0.8 | 9 |
| 28 | Design of a Highly Robust Triple-Node-Upset Self-Recoverable Latch. IEEE Access, 2021, 9, 113622-113630. | 4.2 | 9 |
| 29 | Anti-interference low-power double-edge triggered flip-flop based on C-elements. Tsinghua Science and Technology, 2022, 27, 1-12. | 6.1 | 8 |
| 30 | Design of Low-Power WiNoC with Congestion-Aware Wireless Node. Journal of Circuits, Systems and Computers, 2018, 27, 1850148. | 1.5 | 7 |
| 31 | Chip test pattern reordering method using adaptive test to reduce cost for testing of ICs. IEICE Electronics Express, 2021, 18, 20200420-20200420. | 0.8 | 7 |
| 32 | TPDICE and Sim Based 4-Node-Upset Completely Hardened Latch Design for Highly Robust Computing in Harsh Radiation. , 2021, , . | | 7 |
| 33 | A Lightweight Configurable XOR RO-PUF Design Based on Xilinx FPGA. , 2021, , . | | 7 |
| 34 | Highly Robust Double Node Upset Resilient Hardened Latch Design. IEICE Transactions on Electronics, 2017, E100.C, 496-503. | 0.6 | 6 |
| 35 | An improved communication scheme for non-HOL-blocking wireless NoC. The Integration VLSI Journal, 2018, 60, 240-247. | 2.1 | 6 |
| 36 | An All-Digital and Jitter-Quantizing True Random Number Generator in SRAM-Based FPGAs. , 2018, , . | | 6 |

| # | ARTICLE | IF | CITATIONS |
|----|--|-----|-----------|
| 37 | Novel Application of Deep Learning for Adaptive Testing Based on Long Short-Term Memory. , 2019, , . | | 6 |
| 38 | A transient pulse dually filterable and online self-recoverable latch. IEICE Electronics Express, 2017, 14, 20160911-20160911. | 0.8 | 6 |
| 39 | HLDTL: High-performance, low-cost, and double node upset tolerant latch design. , 2017, , . | | 5 |
| 40 | A single event transient detector in SRAM-based FPGAs. IEICE Electronics Express, 2017, 14, 20170210-20170210. | 0.8 | 5 |
| 41 | Pure Digital Scalable Mixed Entropy Separation Structure for Physical Unclonable Function and True Random Number Generator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1922-1929. | 3.1 | 5 |
| 42 | A Low-Cost High-Efficiency True Random Number Generator on FPGAs. , 2018, , . | | 4 |
| 43 | A Novel Built-In Self-Repair Scheme for 3D Memory. IEEE Access, 2019, 7, 65052-65059. | 4.2 | 4 |
| 44 | A Nanofluidic Sensor for Real-Time Detection of Ultratrace Contaminant Particles in IC Fabrication. IEEE Sensors Journal, 2021, 21, 755-764. | 4.7 | 4 |
| 45 | A high performance SEU-tolerant latch for nanoscale CMOS technology. , 2014, , . | | 4 |
| 46 | Design of Wireless Network on Chip with Priority-Based MAC. Journal of Circuits, Systems and Computers, 2019, 28, 1950124. | 1.5 | 3 |
| 47 | A high performance SEU-tolerant latch for nanoscale CMOS technology. , 2014, , . | | 2 |
| 48 | A Hybrid DMR Latch to Tolerate MNU Using TDICE and WDICE. , 2018, , . | | 2 |
| 49 | A Dynamic Self-Adaptive Correction Method for Error Resilient Application. , 2013, , . | | 1 |
| 50 | Novel approach of LSTM for adaptive testing. , 2019, , . | | 1 |
| 51 | Cross-Layer Dual Modular Redundancy Hardened Scheme of Flip-Flop Design Based on Sense-Amplifier. Journal of Circuits, Systems and Computers, 2021, 30, 2120003. | 1.5 | 1 |
| 52 | An improved aging-predict scheme based on symmetrical nor gate. Journal of Electronics, 2013, 30, 509-516. | 0.2 | 0 |
| 53 | A fault detection sensor for circuit aging using double-edge-triggered flip-flop. Journal of Electronics, 2013, 30, 97-103. | 0.2 | 0 |
| 54 | NBTI mitigation by M-IVC with input duty cycle and randomness constraints. , 2016, , . | | 0 |

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|----|---|----|-----------|
| 55 | Co-mitigating circuit PBTI and HCI aging considering NMOS transistor stacking effect. , 2016, , . | | 0 |
| 56 | Two 0.8 V, Highly Reliable RHBD 10T and 12T SRAM Cells for Aerospace Applications. , 2022, , . | | 0 |