

Rajit Manohar

List of Publications by Year in Descending Order

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

45
papers

2,941
citations

11
h-index

54
g-index

54
ext. papers

3,895
ext. citations

4
avg, IF

4.52
L-index

#	Paper	IF	Citations
45	General Approach to Asynchronous Circuits Simulation Using Synchronous FPGAs. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2021 , 1-1	2.5	
44	An Open-Source EDA Flow for Asynchronous Logic. <i>IEEE Design and Test</i> , 2021 , 38, 27-37	1.4	1
43	Balancing Specialized Versus Flexible Computation in Brain-Computer Interfaces. <i>IEEE Micro</i> , 2021 , 41, 87-94	1.8	1
42	Pilot Evaluations of Two Bluetooth Contact Tracing Approaches on a University Campus: Mixed Methods Study. <i>JMIR Formative Research</i> , 2021 , 5, e31086	2.5	1
41	Exact Timing Analysis for Asynchronous Circuits With Multiple Periods. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2020 , 39, 3134-3138	2.5	1
40	A Systematic Approach for Arbitration Expressions. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2020 , 67, 4960-4969	3.9	1
39	2020 ,		3
38	Hardware-Software Co-Design for Brain-Computer Interfaces 2020 ,		5
37	Self-Timed Adaptive Digit-Serial Addition. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2019 , 27, 2131-2141	2.6	0
36	Operation-Dependent Frequency Scaling Using Desynchronization. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2019 , 27, 799-809	2.6	3
35	Asynchronous Signalling Processes 2019 ,		3
34	SPRoute: A Scalable Parallel Negotiation-based Global Router 2019 ,		2
33	AMC: An Asynchronous Memory Compiler 2019 ,		4
32	Braindrop: A Mixed-Signal Neuromorphic Architecture With a Dynamical Systems-Based Programming Model. <i>Proceedings of the IEEE</i> , 2019 , 107, 144-164	14.3	73
31	QDI Constant-Time Counters. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2019 , 27, 83-91	2.6	1
30	A Continuous-Time Digital IIR Filter With Signal-Derived Timing and Fully Agile Power Consumption. <i>IEEE Journal of Solid-State Circuits</i> , 2018 , 53, 418-430	5.5	7
29	Exact Timing Analysis for Asynchronous Systems. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2018 , 37, 203-216	2.5	7

28	On Using Time Without Clocks via Zigzag Causality 2017 ,		5
27	The Eventual C-Element Theorem for Delay-Insensitive Asynchronous Circuits 2017 ,		5
26	Gradual Synchronization 2016 ,		4
25	Automatic obfuscated cell layout for trusted split-foundry design 2015 ,		18
24	Comparing Stochastic and Deterministic Computing. <i>IEEE Computer Architecture Letters</i> , 2015 , 14, 119-128		13
23	AES Hardware-Software Co-design in WSN 2015 ,		5
22	TrueNorth: Design and Tool Flow of a 65 mW 1 Million Neuron Programmable Neurosynaptic Chip. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2015 , 34, 1537-1557	2.5	530
21	Analyzing Isochronic Forks with Potential Causality 2015 ,		6
20	Timing Driven Placement for Quasi Delay-Insensitive Circuits 2015 ,		4
19	Preventing glitches and short circuits in high-level self-timed chip specifications. <i>ACM SIGPLAN Notices</i> , 2015 , 50, 270-279	0.2	
18	ULSNAP: An ultra-low power event-driven microcontroller for sensor network nodes 2014 ,		6
17	Artificial brains. A million spiking-neuron integrated circuit with a scalable communication network and interface. <i>Science</i> , 2014 , 345, 668-73	33.3	2012
16	cellTK: Automated Layout for Asynchronous Circuits with Nonstandard Cells 2013 ,		11
15	A memory-efficient routing method for large-scale spiking neural networks 2013 ,		9
14	An Asynchronous Floating-Point Multiplier 2012 ,		5
13	Address-Event Communication Using Token-Ring Mutual Exclusion 2011 ,		10
12	An Operand-Optimized Asynchronous IEEE 754 Double-Precision Floating-Point Adder 2010 ,		8
11	Static Power Reduction Techniques for Asynchronous Circuits 2010 ,		11

10	An Asynchronous FPGA with Two-Phase Enable-Scaled Routing 2010 ,			8
9	Reducing Power Consumption with Relaxed Quasi Delay-Insensitive Circuits 2009 ,			5
8	Variability in 3-D integrated circuits 2008 ,			7
7	Utilizing Dynamically Coupled Cores to Form a Resilient Chip Multiprocessor 2007 ,			87
6	Reconfigurable Asynchronous Logic 2006 ,			22
5	An ultra low-power processor for sensor networks. <i>Operating Systems Review (ACM)</i> , 2004 , 38, 27-36	0.8		11
4	Scalable formal design methods for asynchronous VLSI. <i>ACM SIGPLAN Notices</i> , 2002 , 37, 245-246	0.2		
3	Performance and portability of an air quality model. <i>Parallel Computing</i> , 1997 , 23, 2187-2200	1		15
2	Conditional composition. <i>Formal Aspects of Computing</i> , 1995 , 7, 683-703	1.2		2
1	A high-performance asynchronous FPGA: test results			9