Rajit Manohar

List of Publications by Citations

45 papers	2,941 citations	11 h-index	54 g-index
54 ext. papers	3,895 ext. citations	4 avg, IF	4.52 L-index

#	Paper	IF	Citations
45	Artificial brains. A million spiking-neuron integrated circuit with a scalable communication network and interface. *Science*, **2014**, 345, 668-73	33.3	2012
44	TrueNorth: Design and Tool Flow of a 65 mW 1 Million Neuron Programmable Neurosynaptic Chip. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 1537-1557	2.5	530
43	Utilizing Dynamically Coupled Cores to Form a Resilient Chip Multiprocessor **2007**,		87
42	Braindrop: A Mixed-Signal Neuromorphic Architecture With a Dynamical Systems-Based Programming Model. *Proceedings of the IEEE*, **2019**, 107, 144-164	14.3	73
41	Reconfigurable Asynchronous Logic **2006**,		22
40	Automatic obfuscated cell layout for trusted split-foundry design **2015**,		18
39	Performance and portability of an air quality model. *Parallel Computing*, **1997**, 23, 2187-2200	1	15
38	Comparing Stochastic and Deterministic Computing. *IEEE Computer Architecture Letters*, **2015**, 14, 119-122	1.8	13
37	cellTK: Automated Layout for Asynchronous Circuits with Nonstandard Cells **2013**,		11
36	Static Power Reduction Techniques for Asynchronous Circuits **2010**,		11
35	An ultra low-power processor for sensor networks. *Operating Systems Review (ACM)*, **2004**, 38, 27-36	0.8	11
34	Address-Event Communication Using Token-Ring Mutual Exclusion **2011**,		10
33	A memory-efficient routing method for large-scale spiking neural networks **2013**,		9
32	A high-performance asynchronous FPGA: test results		9
31	An Operand-Optimized Asynchronous IEEE 754 Double-Precision Floating-Point Adder **2010**,		8
30	An Asynchronous FPGA with Two-Phase Enable-Scaled Routing **2010**,		8
29	A Continuous-Time Digital IIR Filter With Signal-Derived Timing and Fully Agile Power Consumption. *IEEE Journal of Solid-State Circuits*, **2018**, 53, 418-430	5.5	7

28	Exact Timing Analysis for Asynchronous Systems. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 203-216	2.5	7
27	Variability in 3-D integrated circuits **2008**,		7
26	ULSNAP: An ultra-low power event-driven microcontroller for sensor network nodes **2014**,		6
25	Analyzing Isochronic Forks with Potential Causality **2015**,		6
24	On Using Time Without Clocks via Zigzag Causality **2017**,		5
23	AES Hardware-Software Co-design in WSN **2015**,		5
22	The Eventual C-Element Theorem for Delay-Insensitive Asynchronous Circuits **2017**,		5
21	An Asynchronous Floating-Point Multiplier **2012**,		5
20	Reducing Power Consumption with Relaxed Quasi Delay-Insensitive Circuits **2009**,		5
19	Hardware-Software Co-Design for Brain-Computer Interfaces **2020**,		5
18	Timing Driven Placement for Quasi Delay-Insensitive Circuits **2015**,		4
17	Gradual Synchronization **2016**,		4
16	AMC: An Asynchronous Memory Compiler **2019**,		4
15	Operation-Dependent Frequency Scaling Using Desynchronization. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 799-809	2.6	3
14	Asynchronous Signalling Processes **2019**,		3
13	**2020**,		3
12	Conditional composition. *Formal Aspects of Computing*, **1995**, 7, 683-703	1.2	2
11	SPRoute: A Scalable Parallel Negotiation-based Global Router **2019**,		2

10	Exact Timing Analysis for Asynchronous Circuits With Multiple Periods. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 3134-3138	2.5	1
9	A Systematic Approach for Arbitration Expressions. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2020**, 67, 4960-4969	3.9	1
8	An Open-Source EDA Flow for Asynchronous Logic. *IEEE Design and Test*, **2021**, 38, 27-37	1.4	1
7	Balancing Specialized Versus Flexible Computation in Brain□Computer Interfaces. *IEEE Micro*, **2021**, 41, 87-94	1.8	1
6	Pilot Evaluations of Two Bluetooth Contact Tracing Approaches on a University Campus: Mixed Methods Study. *JMIR Formative Research*, **2021**, 5, e31086	2.5	1
5	QDI Constant-Time Counters. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 83-91	2.6	1
4	Self-Timed Adaptive Digit-Serial Addition. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 2131-2141	2.6	0
3	Scalable formal design methods for asynchronous VLSI. *ACM SIGPLAN Notices*, **2002**, 37, 245-246	0.2	
2	General Approach to Asynchronous Circuits Simulation Using Synchronous FPGAs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	
1	Preventing glitches and short circuits in high-level self-timed chip specifications. *ACM SIGPLAN Notices*, **2015**, 50, 270-279	0.2	