

Maurizio Zamboni

List of Publications by Year in descending order

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64
docs citations

64
times ranked

588
citing authors

#	ARTICLE	IF	CITATIONS
1	Towards Compact Modeling of Noisy Quantum Computers: A Molecular-Spin-Qubit Case of Study. ACM Journal on Emerging Technologies in Computing Systems, 2022, 18, 1-26.	1.8	4
2	Octantis: An Exploration Tool for Beyond von Neumann architectures. , 2021, , .		0
3	Hybrid-SIMD: a Modular and Reconfigurable approach to Beyond von Neumann Computing. IEEE Transactions on Computers, 2021, , 1-1.	2.4	1
4	Data Processing and Information Classification An In-Memory Approach. Sensors, 2020, 20, 1681.	2.1	2
5	ToPoliNano: A CAD Tool for Nano Magnetic Logic. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1061-1074.	1.9	40
6	NANOcom: A Mosaic Approach for nanoelectronic circuits design. , 2017, , .		0
7	Design of MRAM-Based Magnetic Logic Circuits. IEEE Nanotechnology Magazine, 2017, 16, 851-859.	1.1	6
8	3D design of a pNML random access memory. , 2017, , .		7
9	Domain Wall Interconnections for NML. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 3067-3076.	2.1	0
10	Reconfigurable Systolic Array: From Architecture to Physical Design for NML. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3208-3217.	2.1	18
11	Virtual Clocking for NanoMagnet Logic. IEEE Nanotechnology Magazine, 2016, 15, 962-970.	1.1	21
12	Modeling, Design, and Analysis of MagnetoElastic NML Circuits. IEEE Nanotechnology Magazine, 2016, 15, 977-985.	1.1	7
13	Feedbacks in QCA: A Quantitative Approach. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2233-2243.	2.1	28
14	Interleaving in Systolic-Arrays: A Throughput Breakthrough. IEEE Transactions on Computers, 2015, 64, 1940-1953.	2.4	5
15	Protein Alignment Systolic Array Throughput Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 68-77.	2.1	12
16	A Joint Source/Channel Approach to Strengthen Embedded Programmable Devices against Flash Memory Errors. IEEE Embedded Systems Letters, 2014, 6, 77-80.	1.3	7
17	Nanoarray architectures multilevel simulation. ACM Journal on Emerging Technologies in Computing Systems, 2014, 10, 1-20.	1.8	3
18	Magnetoelastic Clock System for Nanomagnet Logic. IEEE Nanotechnology Magazine, 2014, 13, 963-973.	1.1	34

#	ARTICLE	IF	CITATIONS
19	ToPoliNano: NanoMagnet Logic Circuits Design and Simulation. Lecture Notes in Computer Science, 2014, , 274-306.	1.0	7
20	Simulation and design of an UWB imaging system for breast cancer detection. The Integration VLSI Journal, 2014, 47, 548-559.	1.3	13
21	A quantitative approach to testing in Quantum dot Cellular Automata: NanoMagnet Logic case. , 2014, , .		15
22	Enabling design and simulation of massive parallel nanoarchitectures. Journal of Parallel and Distributed Computing, 2014, 74, 2530-2541.	2.7	16
23	UWB microwave imaging for breast cancer detection. Transactions on Embedded Computing Systems, 2014, 13, 1-22.	2.1	146
24	NanoMagnet Logic: An Architectural Level Overview. Lecture Notes in Computer Science, 2014, , 223-256.	1.0	10
25	Electric Clock for NanoMagnet Logic Circuits. Lecture Notes in Computer Science, 2014, , 73-110.	1.0	8
26	NanoMagnet Logic: An Architectural Level Overview. Lecture Notes in Computer Science, 2014, , 223-256.	1.0	16
27	ToPoliNano: NanoMagnet Logic Circuits Design and Simulation. Lecture Notes in Computer Science, 2014, , 274-306.	1.0	16
28	Electric Clock for NanoMagnet Logic Circuits. Lecture Notes in Computer Science, 2014, , 73-110.	1.0	5
29	Nanomagnetic Logic Microprocessor: Hierarchical Power Model. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1410-1420.	2.1	26
30	LAURA-NoC: Local Automatic Rate Adjustment in Network-on-Chips With a Simple DVFS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 647-651.	2.2	10
31	UWB receiver for breast cancer detection: Comparison between two different approaches. , 2013, , .		3
32	Breast cancer detection based on an UWB imaging system: Receiver design and simulations. , 2013, , .		3
33	Hardware Acceleration of Beamforming in a UWB Imaging Unit for Breast Cancer Detection. VLSI Design, 2013, 2013, 1-11.	0.5	6
34	A Hardware Viewpoint on Biosequence Analysis. ACM Journal on Emerging Technologies in Computing Systems, 2013, 9, 1-21.	1.8	13
35	Power-gating technique for network-on-chip buffers. Electronics Letters, 2013, 49, 1438-1440.	0.5	13
36	Majority Voter Full Characterization for Nanomagnet Logic Circuits. IEEE Nanotechnology Magazine, 2012, 11, 940-947.	1.1	45

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37	DVFS Based on Voltage Dithering and Clock Scheduling for GALS Systems. , 2012, , .		11
38	An NCL-HDL Snake-Clock-Based Magnetic QCA Architecture. IEEE Nanotechnology Magazine, 2011, 10, 1141-1149.	1.1	65
39	Nanofabric power analysis: Biosequence alignment case study. , 2011, , .		7
40	Asynchrony in Quantum-Dot Cellular Automata Nanocomputation: Elixir or Poison?. IEEE Design and Test of Computers, 2011, 28, 72-83.	1.4	31
41	A NoC-based hybrid message-passing/shared-memory approach to CMP design. Microprocessors and Microsystems, 2011, 35, 261-273.	1.8	14
42	Asynchronous Solutions for Nanomagnetic Logic Circuits. ACM Journal on Emerging Technologies in Computing Systems, 2011, 7, 1-18.	1.8	20
43	MEDEA: a hybrid shared-memory/message-passing multiprocessor NoC-based architecture. , 2010, , .		21
44	A flexible simulation methodology and tool for nanoarray-based architectures. , 2010, , .		16
45	A Fully Differential Digital CMOS UWB Pulse Generator. Circuits, Systems, and Signal Processing, 2009, 28, 649-664.	1.2	9
46	A mixed-signal demodulator for a low-complexity IR-UWB receiver: Methodology, simulation and design. The Integration VLSI Journal, 2009, 42, 47-60.	1.3	5
47	A Case Study for NoC-Based Homogeneous MPSoC Architectures. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 384-388.	2.1	23
48	A 1-bit Synchronization Algorithm for a Reduced Complexity Energy Detection UWB Receiver. , 2007, , .		2
49	An effective AMS Top-Down Methodology Applied to the Design of a Mixed-Signal UWB System-on-Chip. , 2007, , .		2
50	The NoCray Graphic Accelerator: a Case-study for MP-SoC Network-on-Chip Design Methodology. , 2007, , .		2
51	A Low-power CMOS 2-PPM Demodulator for Energy Detection IR-UWB Receivers. , 2007, , .		4
52	Effects of temperature in deep-submicron global interconnect optimization in future technology nodes. Microelectronics Journal, 2004, 35, 849-857.	1.1	4
53	An electromigration and thermal model of power wires for a priori high-level reliability prediction. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2004, 12, 349-358.	2.1	16
54	Novel JPEG 2000 Compliant DWT and IWT VLSI Implementations. Journal of Signal Processing Systems, 2003, 35, 137-153.	1.0	16

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55	Coupled electro-thermal modeling and optimization of clock networks. <i>Microelectronics Journal</i> , 2003, 34, 1175-1185.	1.1	1
56	Architectural strategies for low-power VLSI turbo decoders. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2002, 10, 279-285.	2.1	36
57	Power Supply Design Parameters for Switching-Noise Control in Deep-Submicron Circuits Design Flows. <i>Analog Integrated Circuits and Signal Processing</i> , 2002, 31, 225-248.	0.9	2
58	VLSI architectures for turbo codes. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 1999, 7, 369-379.	2.1	109
59	A comprehensive submicrometer MOST delay model and its application to CMOS buffers. <i>IEEE Journal of Solid-State Circuits</i> , 1997, 32, 1254-1262.	3.5	19
60	PROXIMA: PROlog eXecutlon MACHine. <i>IEEE Journal of Solid-State Circuits</i> , 1993, 28, 362-370.	3.5	0
61	Space and time redundancy in microcomputer bus communication. <i>Computer Standards and Interfaces</i> , 1988, 7, 233-246.	3.8	0
62	Design considerations on a VLSI Prolog interpreter. <i>Microprocessing and Microprogramming</i> , 1987, 21, 267-273.	0.3	0
63	Monitoring tools for multiprocessors. <i>Microprocessing and Microprogramming</i> , 1986, 18, 409-416.	0.3	12
64	Magnetic QCA Design: Modeling, Simulation and Circuits. , 0, , .		7