Antonio Petraglia

List of Publications by Year in descending order

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#	Article	IF	CITATIONS
1	Ultra-Low-Power CMOS Voltage Reference Topologies Regarding Technology Node. , 2022, , .		2
2	Convolutional Neural Networks for Underwater Pipeline Segmentation using Imperfect Datasets. , 2021, , .		0
3	A Three-Stage Charge Pump with Forward Body Biasing in 28 nm UTBB FD-SOI CMOS. , 2021, , .		5
4	A 120 mV Supply, Triode-Regulated Femto-Watt CMOS Voltage Reference Design. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 587-591.	3.0	4
5	A Three-Stage Charge Pump With Forward Body Biasing in 28 nm UTBB FD-SOI CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4810-4819.	5.4	6
6	Adjustable Output CMOS Voltage Reference Design. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1690-1694.	3.0	14
7	Closed-Form Analysis of Metastability Voltage in 28-nm UTBB FD-SOI CMOS Technology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 625-629.	3.0	Ο
8	Underwater Acoustic Channel Estimation and Equalization via Adaptive Filtering and Sparse Approximation. , 2019, , .		2
9	CMOS Switched-Capacitor DSB-SSB Converter Using a Hilbert Transformer. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1494-1498.	3.0	Ο
10	Static noise margin trade-offs for 6T-SRAM cell sizing in 28†nm UTBB FD-SOI CMOS technology. Microelectronics Journal, 2018, 78, 94-100.	2.0	4
11	Performance of analogue, digital and hybrid finite impulse response filter banks affected by realisation errors and noise. IET Signal Processing, 2018, 12, 949-956.	1.5	0
12	Comparison of CNN and MLP classifiers for algae detection in underwater pipelines. , 2017, , .		12
13	Second-order analog filter sections with independently tunable center frequency and bandwidth. , 2017, , .		Ο
14	A Computer-Aided Approach for Voltage Reference Circuit Design. Analog Integrated Circuits and Signal Processing, 2016, 89, 511-520.	1.4	5
15	Accurate Electrothermal Modeling of Thermoelectric Generators. , 2015, , .		7
16	A computer-aided approach for voltage reference circuit design. , 2015, , .		2
17	CMOS Imager With Focal-Plane Analog Image Compression Combining DPCM and VQ. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 1331-1344.	5.4	29
18	A CMOS imaging system featuring focal-plane compression based on DPCM and VQ. , 2012, , .		4

A CMOS imaging system featuring focal-plane compression based on DPCM and VQ. , 2012, , . 18

ANTONIO PETRAGLIA

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19	Current-mode analog integrated circuit for focal-plane image compression. , 2012, , .		1
20	A Fully Differential CMOS Voltage Buffer forÂContinuous- and Discrete-Time Applications. Circuits, Systems, and Signal Processing, 2011, 30, 355-370.	2.0	1
21	A circuit for focal-plane image compression using vector quantization. , 2011, , .		4
22	Using a Genetic Algorithm to Optimize Capacitance Ratio Approximations in SC Filters. Circuits, Systems, and Signal Processing, 2010, 29, 687-707.	2.0	1
23	Optimizing Capacitance Ratio Assignment for Low-Sensitivity SC Filter Implementation. IEEE Transactions on Evolutionary Computation, 2010, 14, 375-380.	10.0	5
24	Frequency Domain FIR Filter Design Using Fuzzy Adaptive Simulated Annealing. Circuits, Systems, and Signal Processing, 2009, 28, 899.	2.0	35
25	An approximation algorithm to improve capacitance matching in the design of SC filters. Analog Integrated Circuits and Signal Processing, 2008, 57, 49-56.	1.4	2
26	Analog inner product operations for image compression in 0.35-μm CMOS. Analog Integrated Circuits and Signal Processing, 2008, 57, 141-150.	1.4	2
27	A 0.35Âμm CMOS AM demodulator. Analog Integrated Circuits and Signal Processing, 2008, 57, 89-96.	1.4	0
28	Introduction to the special issue on the SBCCI 2007. Analog Integrated Circuits and Signal Processing, 2008, 57, 1-2.	1.4	1
29	New Error Sensitivity Model for the Analog Hardware Implementation of Inner Products. , 2006, , .		2