Maksim Jenihhin

List of Publications by Year
in descending order

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81	290	1478505	1588992
papers	citations	6	8
		h-index	g-index

83	83	83	126
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Automated Identification of Application-Dependent Safe Faults in Automotive Systems-on-a-Chips. Electronics (Switzerland), 2022, 11, 319.	3.1	2
2	Fast and Fair Computation Offloading Management in a Swarm of Drones Using a Rating-Based Federated Learning Approach. IEEE Access, 2021, 9, 113832-113849.	4.2	7
3	JÃ„NES: A NAS Framework for ML-based EDA Applications. , 2021, , .		1
4	Modeling Soft-Error Reliability Under Variability. , 2021, , .		1
5	A Methodology for Automated Mining of Compact and Accurate Assertion Sets. , 2021, , .		1
6	Calculation of probabilistic testability measures for digital circuits with Structurally Synthesized BDDs. Microprocessors and Microsystems, 2020, 77, 103117.	2.8	2
7	Wafer-Level Die Re-Test Success Prediction Using Machine Learning. , 2020, , .		8
8	Special Session: AutoSoC - A Suite of Open-Source Automotive SoC Benchmarks. , 2020, , .		4
9	A DFT Scheme to Improve Coverage of Hard-to-Detect Faults in FinFET SRAMs. , 2020, , .		4
10	High-Level Combined Deterministic and Pseudo-exhuastive Test Generation for RISC Processors. , 2019, , .		2
11	Modeling Gate-Level Abstraction Hierarchy Using Graph Convolutional Neural Networks to Predict Functional De-Rating Factors. , 2019, , .		6
12	True Path Tracing in Structurally Synthesized BDDs for Testability Analysis of Digital Circuits. , 2019, , .		2
13	Accelerating Transient Fault Injection Campaigns by using Dynamic HDL Slicing. , 2019, , .		3
14	On NBTI-induced Aging Analysis in IEEE 1687 Reconfigurable Scan Networks. , 2019, , .		0
15	PASCAL: Timing SCA Resistant Design and Verification Flow. , 2019, , .		5
16	Challenges of Reliability Assessment and Enhancement in Autonomous Systems. , 2019, , .		8
17	Energy-Efficient Multi-fragment Markov Model Guided Online Model-Based Testing for MPSoC. Studies in Systems, Decision and Control, 2019, , 273-297.	1.0	0
18	Fast identification of true critical paths in sequential circuits. Microelectronics Reliability, 2018, 81, 252-261.	1.7	2

#	Article	IF	Citations
19	Hierarchical Timing-Critical Paths Analysis in Sequential Circuits. , 2018, , .		1
20	RESCUE: Cross-Sectoral PhD Training Concept for Interdependent Reliability, Security and Quality. , 2018, , .		1
21	Upgrading QoSinNoC: Efficient Routing for Mixed-Criticality Applications and Power Analysis. , 2018, , .		0
22	Multi-view modeling for MPSoC design aspects. , 2018, , .		0
23	Towards Multidimensional Verification: Where Functional Meets Non-Functional. , 2018, , .		8
24	QoSinNoC: Analysis of QoS-Aware NoC Architectures for Mixed-Criticality Applications. , 2018, , .		5
25	Software-Level TMR Approach for On-Board Data Processing in Space Applications. , 2018, , .		1
26	Timing-critical path analysis with structurally synthesized BDDs. , 2018, , .		0
27	Designing Reliable Cyber-Physical Systems. Lecture Notes in Electrical Engineering, 2018, , 15-38.	0.4	2
28	BASTION: Board and SoC test instrumentation for ageing and no failure found. , 2017, , .		1
29	A scalable technique to identify true critical paths in sequential circuits. , 2017, , .		1
30	Designing reliable cyber-physical systems overview associated to the special session at FDL'16. , 2016, , .		1
31	Rejuvenation of NBTI-Impacted Processors Using Evolutionary Generation of Assembler Programs. , 2016, , .		4
32	Universal mitigation of NBTI-induced aging by design randomization. , 2016, , .		0
33	Identification and Rejuvenation of NBTI-Critical Logic Paths in Nanoscale Circuits. Journal of Electronic Testing: Theory and Applications (JETTA), 2016, 32, 273-289.	1.2	16
34	Gate-level modelling of NBTI-induced delays under process variations. , 2016, , .		4
35	Rejuvenation of nanoscale logic at NBTI-critical paths using evolutionary TPG. , 2015, , .		2
36	SPICE-Inspired Fast Gate-Level Computation of NBTI-induced Delays in Nanoscale Logic. , 2015, , .		7

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37	SystemC-Based Loose Models for Simulation Speed-Up by Abstraction of RTL IP Cores. , 2015, , .		0
38	FSMD RTL design manipulation for clock interface abstraction. , 2015, , .		0
39	Automated Design Error Localization in RTL Designs. IEEE Design and Test, 2014, 31, 83-92.	1.2	8
40	Hierarchical identification of NBTI-critical gates in nanoscale logic. , 2014, , .		9
41	Abstraction of clock interface for conversion of RTL VHDL to SystemC. , 2014, , .		2
42	Diagnostic Test Generation for Statistical Bug Localization Using Evolutionary Computation. Lecture Notes in Computer Science, 2014, , 425-436.	1.3	0
43	Extensible open-source framework for translating RTL VHDL IP cores to SystemC. , 2013, , .		2
44	Identifying NBTI-Critical Paths in Nanoscale Logic. , 2013, , .		4
45	Assessment of diagnostic test for automated bug localization. , 2013, , .		1
46	Automated design error debug using high-level decision diagrams and mutation operators. Microprocessors and Microsystems, 2013, 37, 505-513.	2.8	3
47	Performance analysis of cosimulating processor core in VHDL and SystemC. , 2013, , .		0
48	Diagnostic Modeling of Digital Systems with Multi-Level Decision Diagrams. , 2013, , 407-433.		1
49	Foreword to the 15th IEEE DDECS Symposium. , 2012, , .		0
50	A scalable model based RTL framework zamiaCAD for static analysis. , 2012, , .		0
51	On the Reuse of TLM Mutation Analysis at RTL. Journal of Electronic Testing: Theory and Applications (JETTA), 2012, 28, 435-448.	1.2	3
52	Identifying Untestable Faults in Sequential Circuits Using Test Path Constraints. Journal of Electronic Testing: Theory and Applications (JETTA), 2012, 28, 511-521.	1.2	2
53	Diagnosis and correction of multiple design errors using critical path tracing and mutation analysis. , 2012, , .		1
54	A scalable model based RTL framework zamiaCAD for static analysis. , 2012, , .		10

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55	Combining dynamic slicing and mutation operators for ESL correction. , 2012, , .		18
56	Localization of Bugs in Processor Designs Using zamiaCAD Framework. , 2012, , .		4
57	PSL assertion checkers synthesis with ASM based HLS tool ABELITE. , 2012, , .		2
58	Automated test bench generation for high-level synthesis flow ABELITE. , 2011, , .		0
59	Mutation analysis for SystemC designs at TLM. , 2011, , .		8
60	Constraint-Based Hierarchical Untestability Identification for Synchronous Sequential Circuits. , 2011, , .		7
61	Constraint-based test pattern generation at the Register-Transfer Level. , 2010, , .		6
62	Mutation analysis with high-level decision diagrams. , 2010, , .		2
63	An approach for PSL assertion coverage analysis with high-level decision diagrams. , 2010, , .		1
64	High-level design error diagnosis using backtrace on decision diagrams. , 2010, , .		2
65	PSL Assertion Checking Using Temporally Extended High-Level Decision Diagrams. Journal of Electronic Testing: Theory and Applications (JETTA), 2009, 25, 289-300.	1.2	7
66	High-Level Decision Diagrams based coverage metrics for verification and test. , 2009, , .		4
67	Mixed hierarchical-functional fault models for targeting sequential cores. Journal of Systems Architecture, 2008, 54, 465-477.	4.3	6
68	Code Coverage Analysis using High-Level Decision Diagrams. , 2008, , .		8
69	Temporally Extended High-Level Decision Diagrams for PSL Assertions Simulation. , 2008, , .		5
70	APRICOT: A framework for teaching digital systems verification. , 2008, , .		1
71	High-level decision diagram manipulations for code coverage analysis. , 2008, , .		5
72	On reusability of verification assertions for testing. , 2008, , .		0

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73	Hierarchical Calculation of Malicious Faults for Evaluating the Fault-Tolerance. , 2008, , .		3
74	Hierarchical Analysis of Short Defects between Metal Lines in CMOS IC. , 2008, , .		4
75	Layout to Logic Defect Analysis for Hierarchical Test Generation. , 2007, , .		1
76	Test Time Minimization for Hybrid BIST of Core-Based Systems. Journal of Computer Science and Technology, 2006, 21, 907-912.	1.5	7
77	TTBist: a DfT Tool for Enhancing Functional Test for SoC. International Biennial Baltic Electronics Conference, 2006, , .	0.0	1
78	Test time minimization for hybrid BIST of core-based systems. , 2003, , .		21
79	Hybrid BIST Optimization for Core-based Systems with Test Pattern Broadcasting. , 0, , .		1
80	Diagnostic Modeling of Digital Systems with Multi-Level Decision Diagrams. Advances in Computer and Electrical Engineering Book Series, 0, , 92-118.	0.3	6
81	High-Level Decision Diagram Simulation for Diagnosis and Soft-Error Analysis. Advances in Computer and Electrical Engineering Book Series, 0, , 294-309.	0.3	2