Hong-June Park

List of Publications by Year
in descending order

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81 papers	1,272 citations	430874 18 h-index	395702 33 g-index
81 all docs	81 docs citations	81 times ranked	1066 citing authors

#	Article	IF	Citations
1	A DFE-Enhanced Phase-Difference Modulation Signaling for Multi-Drop Memory Interfaces. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1862-1866.	3.0	1
2	A Duo-Binary Transceiver With Time-Based Receiver and Voltage-Mode Time-Interleaved Mixing Transmitter for DRAM Interface. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2409-2413.	3.0	3
3	A 7.8-Gb/s 2.9-pJ/b Single-Ended Receiver With 20-Tap DFE for Highly Reflective Channels. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 818-822.	3.1	8
4	A Body Channel Communication Technique Utilizing Decision Feedback Equalization. IEEE Access, 2020, 8, 198468-198481.	4.2	6
5	Low-Power Small-Area Inverter-Based DSM for MEMS Microphone. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2392-2396.	3.0	1
6	A 7.8 Gb/s/pin, 1.96 pJ/b Transceiver With Phase-Difference-Modulation Signaling for Highly Reflective Interconnects. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 2114-2127.	5.4	5
7	An 18-Gb/s NRZ Transceiver With a Channel-Included 2-UI Impulse-Response Filtering FFE and 1-Tap DFE Compensating up to 32-dB Loss. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2863-2867.	3.0	6
8	A Multilayer-Learning Current-Mode Neuromorphic System With Analog-Error Compensation. IEEE Transactions on Biomedical Circuits and Systems, 2019, 13, 986-998.	4.0	4
9	A Quadrature RC Oscillator With Noise Reduction by Voltage Swing Control. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3077-3088.	5.4	12
10	Introduction to the Special Section on the 2018 Asian Solid-State Circuits Conference (A-SSCC). IEEE Journal of Solid-State Circuits, 2019, 54, 2635-2636.	5.4	0
11	A 192-pW Voltage Reference Generating Bandgapâ€“$V_{ext{th}}$ With Process and Temperature Dependence Compensation. IEEE Journal of Solid-State Circuits, 2019, 54, 3281-3291.	5.4	46
12	A 0.0043-mm² 0.3â€“1.2-V Frequency-Scalable Synthesized Fractional-N Digital PLL With a Speculative Dual-Referenced Interpolating TDC. IEEE Journal of Solid-State Circuits, 2019, 54, 99-108.	5.4	16
13	Parallel Branching of Two 2-DIMM Sections With Write-Direction Impedance Matching for an 8-Drop 6.4-Gb/s SDRAM Interface. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 336-342.	2.5	4
14	A 9.3 nW all-in-one bandgap voltage and current reference circuit using leakage-based PTAT generation and DIBL characteristic. , 2018, , .		5
15	An On-Chip Learning Neuromorphic Autoencoder With Current-Mode Transposable Memory Read and Virtual Lookup Table. IEEE Transactions on Biomedical Circuits and Systems, 2018, 12, 161-170.	4.0	15
16	An 84.6-dB-SNDR and 98.2-dB-SFDR Residue-Integrated SAR ADC for Low-Power Sensor Applications. IEEE Journal of Solid-State Circuits, 2018, 53, 404-417.	5.4	24
17	A low-power wide dynamic-range current readout circuit for biosensors. , 2018, , .		0
18	A 7.8Gb/s/pin 1.96pJ/b compact single-ended TRX and CDR with phase-difference modulation for highly reflective memory interfaces. , 2018, , .		10

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19	An FFE Transmitter Which Automatically and Adaptively Relaxes Impedance Matching. IEEE Journal of Solid-State Circuits, 2018, 53, 1780-1792.	5.4	12
20	A Time-Based Receiver With 2-Tap Decision Feedback Equalizer for Single-Ended Mobile DRAM Interface. IEEE Journal of Solid-State Circuits, 2018, 53, 144-154.	5.4	13
21	A Search Algorithm for the Worst Operation Scenario of a Cross-Point Phase-Change Memory Utilizing Particle Swarm Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2591-2598.	3.1	3
22	A Study on Bandgap Reference Circuit With Leakage-Based PTAT Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2310-2321.	3.1	11
23	A 250- $muext{W}$ 2.4-GHz Fast-Lock Fractional-N Frequency Generation for Ultralow-Power Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 106-110.	3.0	7
24	An Approximate Transfer Function Model of Two Serially Connected Heterogeneous Transmission Lines. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1067-1071.	3.0	2
25	23.7 A time-based receiver with 2-tap DFE for a 12Gb/s/pin single-ended transceiver of mobile DRAM interface in 0.8V 65nm CMOS. , 2017, , .		6
26	5.5 A quadrature relaxation oscillator with a process-induced frequency-error compensation loop. , 2017, , .		24
27	A Self-Biased Current-Mode Amplifier With an Application to 10-bit Pipeline ADC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1706-1717.	5.4	7
28	Investigation on the Worst Read Scenario of a ReRAM Crossbar Array. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2402-2410.	3.1	6
29	All-Synthesizable Current-Mode Transmitter Driver for USB2.0 Interface. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 788-792.	3.1	4
30	A 10-GHz multi-purpose reconfigurable built-in self-test circuit for high-speed links. , 2017, , .		5
31	All-synthesizable 6Gbps voltage-mode transmitter for serial link. , 2016, , .		0
32	An ECG monitoring system using android smart phone. , 2016, , .		3
33	A low-power LDO circuit with a fast load regulation. , 2016, , .		3
34	A Coefficient-Error-Robust Feed-Forward Equalizing Transmitter for Eye-Variation and Power Improvement. IEEE Journal of Solid-State Circuits, 2016, 51, 1902-1914.	5.4	5
35	A 0.65-to-10.5 Gb/s Reference-Less CDR With Asynchronous Baud-Rate Sampling for Frequency Acquisition and Adaptive Equalization. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 276-287.	5.4	19
36	A reduced-size look-up-table for ADC sample-times of a single-chip non-uniform-sampling digital-beamformer for ultrasound medical imaging. , 2015, , .		1

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37	An Approximate Closed-Form Transfer Function Model for Diverse Differential Interconnects. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 1335-1344.	5.4	12
38	Analytical Formulas for Tradeoff Among Channel Loss, Length, and Frequency of <inline-formula> <tex-math notation="LaTeX">RC </tex-math></inline-formula>- and <inline-formula> <tex-math notation="LaTeX">LC </tex-math></inline-formula>-Dominant Single-Ended Interconnects for Fast Equalized Link Tradeoff Estimation. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2015, 5, 1497-1506.	2.5	3
39	A 40-mV-Swing Single-Ended Transceiver for TSV with a Switched-Diode RX Termination. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 987-991.	3.0	6
40	An open-loop differential time amplifier. , 2014, , .		0
41	Analysis of an Open-Loop Time Amplifier With a Time Gain Determined by the Ratio of Bias Current. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 481-485.	3.0	21
42	An 80 mV-Swing Single-Ended Duobinary Transceiver With a TIA RX Termination for the Point-to-Point DRAM Interface. IEEE Journal of Solid-State Circuits, 2014, 49, 2618-2630.	5.4	24
43	An Approximate Closed-Form Channel Model for Diverse Interconnect Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 3034-3043.	5.4	11
44	A 0.5-V, 1.47- $muhbox{W}$ 40-kS/s 13-bit SAR ADC With Capacitor Error Compensation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 840-844.	3.0	14
45	Current-Mode Transceiver for Silicon Interposer Channel. IEEE Journal of Solid-State Circuits, 2014, 49, 2044-2053.	5.4	27
46	A 300-MS/s, 1.76-ps-Resolution, 10-b Asynchronous Pipelined Time-to-Digital Converter With on-Chip Digital Background Calibration in 0.13-Âµm CMOS. IEEE Journal of Solid-State Circuits, 2013, 48, 516-526.	5.4	50
47	A 10-bit 25-MS/s 1.25-mW Pipelined ADC With a Semidigital Gm-Based Amplifier. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 142-146.	3.0	6
48	A Digital-Domain Calibration of Split-Capacitor DAC for a Differential SAR ADC Without Additional Analog Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2845-2856.	5.4	83
49	A FIR-Embedded Phase Interpolator Based Noise Filtering for Wide-Bandwidth Fractional-N PLL. IEEE Journal of Solid-State Circuits, 2013, 48, 2795-2804.	5.4	31
50	A QDR-Based 6-GB/s Parallel Transceiver With Current-Regulated Voltage-Mode Output Driver and Byte CDR for Memory Interface. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 91-95.	3.0	4
51	A single-chip time-interleaved 32-channel analog beamformer for ultrasound medical imaging. , 2012, , .		5
52	A spread spectrum clock generator using phase/frequency boosting with a peak power reduction 14.9dB, RMS jitter 1.40ps and power 4.8mW/GHz for USB 3.0. , 2012, , .		0
53	A Transmitter to Compensate for Crosstalk-Induced Jitter by Subtracting a Rectangular Crosstalk Waveform From Data Signal During the Data Transition Time in Coupled Microstrip Lines. IEEE Journal of Solid-State Circuits, 2012, 47, 2068-2079.	5.4	9
54	A 1.9-GHz Fractional-N Digital PLL With Subexponent $ DeltaSigma$ TDC and IIR-Based Noise Cancellation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 721-725.	3.0	3

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55	A fractional-N frequency divider for SSCG using a single dual-modulus integer divider and a phase interpolator. , 2012, , .		5
56	A 1.25 ps Resolution 8b Cyclic TDC in 0.13 mum CMOS. IEEE Journal of Solid-State Circuits, 2012, 47, 736-743.	5.4	68
57	A 2 GHz Fractional-N Digital PLL with 1b Noise Shaping $DeltaSigma$ TDC. IEEE Journal of Solid-State Circuits, 2012, 47, 875-883.	5.4	34
58	5-Gb/s Peak Detector Using a Current Comparator and a Three-State Charge Pump. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 269-273.	3.0	12
59	Phase-blender-based FIR noise filtering techniques for ΔΣ fractional-N PLL. , 2011, , .		0
60	A 2-Gb/s Intrapanel Interface for TFT-LCD With a VSYNC-Embedded Subpixel Clock and a Cascaded Deskew and Multiphase DLL. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 687-691.	3.0	9
61	A high-gain wide-input-range time amplifier with an open-loop architecture and a gain equal to current bias ratio. , 2011, , .		29
62	A 21 fJ/Conversion-Step 100 kS/s 10-bit ADC With a Low-Noise Time-Domain Comparator for Low-Power Sensor Interface. IEEE Journal of Solid-State Circuits, 2011, 46, 651-659.	5.4	139
63	A 110 MHz to 1.4 GHz Locking 40-Phase All-Digital DLL. IEEE Journal of Solid-State Circuits, 2011, 46, 435-444.	5.4	28
64	A Single-Loop SS-LMS Algorithm With Single-Ended Integrating DFE Receiver for Multi-Drop DRAM Interface. IEEE Journal of Solid-State Circuits, 2011, 46, 2053-2063.	5.4	24
65	Digital-domain calibration of split-capacitor DAC with no extra calibration DAC for a differential-type SAR ADC. , 2011, , .		9
66	Serpentine Microstrip Lines With Zero Far-End Crosstalk for Parallel High-Speed DRAM Interfaces. IEEE Transactions on Advanced Packaging, 2010, 33, 552-558.	1.6	37
67	A 1 GHz ADPLL With a 1.25 ps Minimum-Resolution Sub-Exponent TDC in 0.18 mum CMOS. IEEE Journal of Solid-State Circuits, 2010, 45, 2874-2881.	5.4	118
68	A transmitter with different output timing to compensate for the crosstalk-induced jitter of coupled microstrip lines. , 2010, , .		1
69	A 2-Gb/s CMOS Integrating Two-Tap DFE Receiver for Four-Drop Single-Ended Signaling. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 1645-1656.	5.4	14
70	Reduction of Transient Far-End Crosstalk Voltage and Jitter in DIMM Connectors for DRAM Interface. IEEE Microwave and Wireless Components Letters, 2009, 19, 15-17.	3.2	7
71	A 4 Gb/s 3-bit Parallel Transmitter With the Crosstalk-Induced Jitter Compensation Using TX Data Timing Control. IEEE Journal of Solid-State Circuits, 2009, 44, 2891-2900.	5.4	30
72	A CMOS transceiver for DRAM bus system with a demultiplexed equalization scheme. IEEE Journal of Solid-State Circuits, 2002, 37, 245-250.	5.4	11

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73	Empirical equations on electrical parameters of coupled microstrip lines for crosstalk estimation in printed circuit board. IEEE Transactions on Advanced Packaging, 2001, 24, 521-527.	1.6	67
74	A 1-Gb/s bidirectional I/O buffer using the current-mode scheme. IEEE Journal of Solid-State Circuits, 1999, 34, 529-535.	5.4	16
75	SIMULTANEOUS SWITCHING NOISE ANALYSIS OF A 16 MB Ã— 9 DRAM SIMM MEMORY MODULE. Selected Topics in Electornics and Systems, 1996, , 233-254.	0.2	0
76	Empirical equations on electrical parameters of coupled microstrip lines with one side exposed to air. , 0, , .		0
77	A sense amplifier-based CMOS flip-flop with an enhanced output transition time for high-performance microprocessors. , 0, , .		2
78	840 Mb/s CMOS demultiplexed equalizing transceiver for DRAM-to-processer communication. , 0, , .		4
79	A high-speed 50% power-saving half-swing clocking scheme for flip-flop with complementary gate and source drive. , 0, , .		1
80	A mixed-mode single-chip motor-drive-specific microcontroller with a 12-bit 125/KS/s ADC. , 0, , .		1
81	An 8-bit 200 MS/s CMOS folding/interpolating ADC with a reduced number of preamplifiers using an averaging technique. , 0, , .		0