Joao Martino

List of Publications by Year
in descending order

406	1,947	394286 19	454834 30
papers	citations	h-index	g-index

407	407	407	920
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Design of operational transconductance amplifier with Gate-All-Around Nanosheet MOSFET using experimental data from room temperature to 200ÂÂ°C. Solid-State Electronics, 2022, 189, 108238.	0.8	1
2	Trade-off analysis between gm/ID and fT of nanosheet NMOS transistors with different metal gate stack at high temperature. Solid-State Electronics, 2022, 191, 108267.	0.8	0
3	Comparison between Low-Dropout Voltage Regulators Designed with Line and Nanowire Tunnel Field Effect Transistors using Experimental Data. Solid-State Electronics, 2022, , 108328.	0.8	1
4	Signal to noise ratio in nanoscale bioFETs. Solid-State Electronics, 2022, 194, 108358.	0.8	0
5	Voltage gain improvement of the operational transconductance amplifier designed with silicon-on-insulator fin field effect transistor after being exposed to proton-irradiation. Semiconductor Science and Technology, 2021, 36, 035001.	1.0	1
6	Study of a Fringing Field Biosensor Tunnel-FET. ECS Journal of Solid State Science and Technology, 2021, 10, 017004.	0.9	2
7	Study of ^{Î'Î•}SOI MOSFET Reconfigurable Transistor for Biosensing Application. ECS Journal of Solid State Science and Technology, 2021, 10, 027004.	0.9	7
8	Analysis of the ZTC-Point for Vertically Stacked Nanosheet pMOS Devices. , 2021, , .		0
9	Simple Analytical Modelling of an Electronically Tunable Potentiometer and Body Factor Influence. , 2021, , .		0
10	Evaluation of Dielectrically Modulated and Fringing Field Tunneling Field Effect Transistor Biosensors Devices. ECS Journal of Solid State Science and Technology, 2021, 10, 077001.	0.9	1
11	Analog Figures of Merit of Vertically Stacked Silicon Nanosheets nMOSFETs With Two Different Metal Gates for the Sub-7 nm Technology Node Operating at High Temperatures. IEEE Transactions on Electron Devices, 2021, 68, 3630-3635.	1.6	18
12	Current mirror designed with GAA nanosheet MOSFETs from room temperature to 200 Â°C. Semiconductor Science and Technology, 2021, 36, 095019.	1.0	1
13	Study of the UTBB BESOI Tunnel-FET working as a Dual-Technology Transistor. Journal of Integrated Circuits and Systems, 2021, 16, 1-6.	0.3	0
14	Low frequency noise performance of horizontal, stacked and vertical silicon nanowire MOSFETs. Solid-State Electronics, 2021, 184, 108087.	0.8	9
15	Analysis of zero-temperature coefficient behavior on vertically stacked double nanosheet nMOS devices. Microelectronics Journal, 2021, 117, 105277.	1.1	1
16	Gate dielectric material influence on DC behavior of MO(I)SHEMT devices operating up to 150ÂÂ°C. Solid-State Electronics, 2021, 185, 108091.	0.8	4
17	Optimization of a nanoribbon charge-based biosensor using gateless BESOI pMOSFET structure. Solid-State Electronics, 2021, 185, 108076.	0.8	0
18	Impact of gate current on the operational transconductance amplifier designed with nanowire TFETs. Solid-State Electronics, 2021, 186, 108099.	0.8	2

#	Article	IF	Citations
19	High Temperature Influence on the Trade-off between gm/I_D and f_T of nanosheet NMOS Transistors with Different Metal Gate Stack. , 2021, , .		0
20	Improvement of Schottky Junctions for application in BESOI MOSFET. , 2021, , .		0
21	Experimental Analysis of Trade-Off Between Transistor Efficiency and Unit Gain Frequency of Nanosheet NMOS Transistors. , 2021, , .		0
22	Improved Back Enhanced SOI (^{BE}SOI) MOSFET by adding n-doped regions. , 2021, , .		2
23	Impact of Gate Dielectric Material on Basic Parameters of MO(I)SHEMT Devices. ECS Transactions, 2020, 97, 53-58.	0.3	1
24	Proton-Irradiation Influence on Current Mirror Circuit Using Verilog-A Approach Based on Experimental SOI FinFET Characteristics. ECS Transactions, 2020, 97, 171-177.	0.3	0
25	Study of a Charge-Based Biosensor and Reconfigurability using BESOI MOSFET. ECS Transactions, 2020, 97, 115-120.	0.3	1
26	Impact of Schottky contacts on p-type back enhanced SOI MOSFETs. Solid-State Electronics, 2020, 169, 107815.	0.8	3
27	Intrinsic Voltage Gain of Stacked GAA Nanosheet MOSFETs Operating at High Temperatures. ECS Transactions, 2020, 97, 65-69.	0.3	3
28	Readout Circuit Design Using Experimental Data of Line-TFET Devices. ECS Transactions, 2020, 97, 165-170.	0.3	0
29	Operational transconductance amplifier designed with nanowire tunnel-FET with Si, SiGe and Ge sources using experimental data. Semiconductor Science and Technology, 2020, 35, 095020.	1.0	8
30	Analog design with Line-TFET device experimental data: from device to circuit level. Semiconductor Science and Technology, 2020, 35, 055025.	1.0	11
31	Fabrication and Electrical Characterization of Ultra-Thin Body and BOX (UTBB) Back Enhanced SOI (BESOI) pMOSFET. Journal of Integrated Circuits and Systems, 2020, 15, 1-6.	0.3	4
32	Analysis of Omega-Gate Nanowire SOI MOSFET Under Analog Point of View. Journal of Integrated Circuits and Systems, 2020, 15, 1-6.	0.3	0
33	Analysis of the Negative-Bias-Temperature-Instability on Omega-Gate Silicon Nanowire SOI MOSFETs with Different Dimensions. Journal of Integrated Circuits and Systems, 2020, 15, 1-5.	0.3	0
34	Operational Transconductance Amplifier Designed with SiGe-source Nanowire Tunnel-FET using Experimental Lookup Table Model. , 2020, , .		0
35	Comparison between proton irradiated triple gate SOI TFETS and finfets from a TID point of view. Semiconductor Science and Technology, 2019, 34, 065003.	1.0	2
36	Analysis of Omega-Gate Nanowire Devices from Parasitic Conduction to Ionizing Radiation Effects. ECS Journal of Solid State Science and Technology, 2019, 8, Q54-Q60.	0.9	0

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37	Performance evaluation of Tunnel-FET basic amplifier circuits. , 2019, , .		9
38	Double Gate Tunnel-FET Working Like a Permittivity Based Biosensor with Different Drain to Gate and Drain to Biomaterial Alignments. ECS Journal of Solid State Science and Technology, 2019, 8, Q50-Q53.	0.9	13
39	Experimental analysis and improvement of the DC method for self-heating estimation. Solid-State Electronics, 2019, 159, 171-176.	0.8	0
40	Third Generation BESOI (Back-Enhanced SOI) pMOSFET fabricated on UTBB Wafer. , 2019, , .		3
41	Tradeoff between the transistor reconfigurable technology and the zero-temperature-coefficient (ZTC) bias point on BESOI MOSFET. Microelectronics Journal, 2019, 94, 104658.	1.1	7
42	Impact of Drain Doping and Biomaterial Thickness in a Dielectrically Modulated Fringing Field Bio-TFET Device. , 2019, , .		0
43	Silicon Nanowire Tunnel-FET Differential Amplifier Using Verilog-A Lookup Table Approach. , 2019, , .		4
44	Comparison between nMOS and pMOS Î©-gate nanowire down to 10 nm width as a function of back gate bias. Semiconductor Science and Technology, 2019, 34, 035003.	1.0	0
45	Ground Plane Impact on Performance of Relaxed Ge FinFETs. Journal of Integrated Circuits and Systems, 2019, 14, 1-6.	0.3	0
46	OTA Performance Comparison Designed with Experimental NW-MOSFET and NW-TFET Devices. , 2019, , .		2
47	Two-stage amplifier design based on experimental Line-Tunnel FET data. , 2019, , .		1
48	Analysis of proton irradiated n- and p-type strained FinFETs at low temperatures down to 100 K. Semiconductor Science and Technology, 2018, 33, 065003.	1.0	2
49	DC method for self-heating estimation applied to FinFET. , 2018, , .		2
50	Optimization of the permittivity-based BE SOI biosensor. , 2018, , .		8
51	New approach for removing the self-heating from MOSFET current using only DC characteristics. , 2018, , .		0
52	Ground Plane Impact on the Threshold Voltage of Relaxed Ge pFinFETs. , 2018, , .		0
53	Impact of process and device dimensions on Bio-TFET Sensitivity. , 2018, , .		1
54	Optimization of the silicon thickness on Back Enhanced (BE) SOI pMOSFET working as a visible spectrum light sensor. , 2018, , .		7

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55	Back Enhanced SOI MOSFET as UV Light Sensor. , 2018, , .		7
56	Influence of Channel Silicon Thickness and Biological Material Permittivity on nTFET Biosensor. , 2018, , .		1
57	A Tunnel-FET device model based on Verilog-A applied to circuit simulation. , 2018, , .		4
58	Influence of biological element permittivity on BE (Back Enhanced) SOI MOSFETs. , 2018, , .		6
59	Interface Charges Influence on the Subthreshold Region from Triple Gate SOI FinFET to â„¦ -Gate Nanowire Devices. , 2018, , .		2
60	New method for self-heating estimation using only DC measurements. , 2018, , .		1
61	Performance of differential pair circuits designed with line tunnel FET devices at different temperatures. Semiconductor Science and Technology, 2018, 33, 075012.	1.0	5
62	Opposite trends between digital and analog performance for different TFET technologies. , 2018, , .		2
63	Parasitic Conduction on Î©-Gate Nanowires SOI nMOSFETs. ECS Transactions, 2018, 85, 103-109.	0.3	1
64	Impact of Biosensor Permittivity on a Double-Gate nTFET Ambipolar Current. ECS Transactions, 2018, 85, 187-192.	0.3	7
65	Improvement of gm/IDMethod for Detection of Self-Heating Effects. ECS Transactions, 2018, 85, 73-78.	0.3	0
66	Optimization of Source/Drain Schottky Barrier Height on BE SOI MOSFET. ECS Transactions, 2018, 85, 79-84.	0.3	6
67	Total ionizing dose influence on proton irradiated triple gate SOI Tunnel FETs. Journal of Integrated Circuits and Systems, 2018, 13, 1-7.	0.3	1
68	Analysis of current mirror circuits designed with line tunnel FET devices at different temperatures. Semiconductor Science and Technology, 2017, 32, 055015.	1.0	6
69	Analysis of the transistor efficiency of gas phase Zn diffusion In<inf>0.53</inf>Ga<inf>0.47</inf>As nTFETs at different temperatures. , 2017, , .		0
70	The Influence of Oxide Thickness and Indium Amount on the Analog Parameters of In_{<italic>x</italic>}Ga_{1â€“<italic>x</italic>}As nTFETs. IEEE Transactions on Electron Devices, 2017, 64, 3595-3600.	1.6	3
71	Analog parameters on pMOS SOI Î©-gate nanowire down to 10 nm width for different back gate bias. , 2017, , .		2
72	Back Enhanced (BE) SOI MOSFET under non-conventional bias conditions. , 2017, , .		12

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73	Is there a kink effect in FDSOI MOSFETs?. , 2017, , .		3
74	Experimental comparison between relaxed and strained Ge pFinFETs. , 2017, , .		1
75	Low temperature performance of proton irradiated strained SOI FinFET. , 2017, , .		0
76	Study of line-TFET analog performance comparing with other TFET and MOSFET architectures. Solid-State Electronics, 2017, 128, 43-47.	0.8	29
77	Is there a Zero Temperature bias point (ZTC) on Back Enhanced (BE) SOI MOSFET?. , 2017, , .		5
78	Experimental analysis of differential pairs designed with line tunnel FET devices. , 2017, , .		4
79	Reconfigurable back enhanced (BE) SOI MOSFET used to build a logic inverter. , 2017, , .		16
80	Back gate influence on transistor efficiency of SOI nMOS Î©-gate nanowire down to 10nm width. , 2017, , .		1
81	Proton radiation effects on the self-aligned triple gate SOI p-type tunnel FET output characteristic. , 2017, , .		3
82	Simple method for detection of the self-heating signature. , 2017, , .		0
83	Subthreshold region analysis for UTBOX and UTBB SOI nMOSFETs with different channel lengths and silicon thickness. , 2017, , .		0
84	Enhanced model for ZTC in irradiated and strained pFinFET. , 2017, , .		1
85	The influence of low-energy proton irradiaiton on threshold voltage and tranconductance of nanowire SOI n and p-channel transistors. , 2017, , .		0
86	Low temperature influence on long channel STI last process relaxed and strained Ge pFinFETs. , 2017, , .		0
87	Impact of the Zn diffusion process at the source side of In<inf>x</inf>Ga<inf>1â^'x</inf>As nTFETs on the analog parameters down to 10 K. , 2017, , .		0
88	New method for observing self-heating effect using transistor efficiency signature. , 2017, , .		1
89	Analytical Model for Threshold Voltage in UTBB SOI MOSFET in Dynamic Threshold Voltage Operation. Journal of Integrated Circuits and Systems, 2017, 12, 101-106.	0.3	1
90	Zero Temperature Coefficient behavior for advanced MOSFETs. , 2016, , .		9

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91	Back gate bias influence on SOI Î©-gate nanowire down to 10 nm width. , 2016, , .		8
92	n-Channel bulk and DTMOS FinFETs: Investigation of GIDL and gate leakage currents. , 2016, , .		0
93	(Invited) Generation-Recombination Noise in Advanced CMOS Devices. ECS Transactions, 2016, 75, 111-120.	0.3	2
94	Influence of source-drain engineering and temperature on split-capacitance characteristics of FDSOI p-i-n gated diodes. , 2016, , .		0
95	Impact of the low temperature operation on long channel strained Ge pFinFETs fabricated with STI first and last processes. , 2016, , .		2
96	Influence of proton radiation and strain on nFinFET zero temperature coefficient. , 2016, , .		1
97	InGaAs tunnel FET with sub-nanometer EOT and sub-60â€‰mV/dec sub-threshold swing at room temperature. Applied Physics Letters, 2016, 109, .	1.5	48
98	Influence of different UTBB SOI technologies on analog parameters. , 2016, , .		1
99	Split CV mobility at low temperature operation of Ge pFinFETs fabricated with STI first and last processes. Semiconductor Science and Technology, 2016, 31, 114002.	1.0	2
100	DIBL in enhanced dynamic threshold operation of UTBB SOI with different drain engineering at high temperatures. , 2016, , .		0
101	Analysis of TFET and FinFET differential pairs with active load from 300K to 450K. , 2016, , .		1
102	Low frequency noise and fin width study of silicon passivated germanium pFinFETs. , 2016, , .		1
103	Intrinsic voltage gain of Line-TFETs and comparison with other TFET and MOSFET architectures. , 2016, , .		9
104	Effective hole mobility and low-frequency noise characterization of Ge pFinFETs. , 2016, , .		4
105	Body factor scaling in UTBB SOI with supercoupling effect. , 2016, , .		0
106	Comparative study of vertical GAA TFETs and GAA MOSFETs in function of the inversion coefficient. , 2016, , .		2
107	Influence of the Ge amount at source on transistor efficiency of vertical gate all around TFET for different conduction regimes. , 2016, , .		2
108	Impact of the NW-TFET Diameter on the Efficiency and the Intrinsic Voltage Gain From a Conduction Regime Perspective. IEEE Transactions on Electron Devices, 2016, 63, 2930-2935.	1.6	10

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109	Low-Frequency Noise Assessment of Different Ge pFinFET STI Processes. IEEE Transactions on Electron Devices, 2016, 63, 4031-4037.	1.6	8
110	GR-Noise Characterization of Ge pFinFETs With STI First and STI Last Processes. IEEE Electron Device Letters, 2016, 37, 1092-1095.	2.2	9
111	Analog parameters of solid source Zn diffusion In_XGa_{1â^'X}As nTFETs down to 10 K. Semiconductor Science and Technology, 2016, 31, 124001.	1.0	5
112	Low Temperature Effect on Strained and Relaxed Ge pFinFETs STI Last Processes. ECS Transactions, 2016, 75, 213-218.	0.3	3
113	Improved operation of graded-channel SOI nMOSFETs down to liquid helium temperature. Semiconductor Science and Technology, 2016, 31, 114005.	1.0	4
114	Comparative analysis of the intrinsic voltage gain and unit gain frequency between SOI and bulk FinFETs up to high temperatures. Solid-State Electronics, 2016, 123, 124-129.	0.8	7
115	Proton radiation influence on SOI FinFET trade-off between transistor efficiency and unit gain frequency. , 2016, , .		1
116	Back enhanced (BE) SOI pMOSFET behavior at high temperatures. , 2016, , .		5
117	On the assessment of electrically active defects in high-mobility materials and devices. , 2016, , .		0
118	Low-frequency and random telegraph noise performance of Ge-based and IIIâ€“V devices on a Si platform. , 2016, , .		1
119	Impact of In<inf>x</inf>Ga<inf>1â^'x</inf> composition and source Zn diffusion temperature on intrinsic voltage gain in InGaAs TFETs. , 2016, , .		0
120	Ground plane influence on zero-temperature-coefficient in SOI UTBB MOSFETs with different silicon film thicknesses. , 2016, , .		3
121	Analysis of carrier mobility in triple gate SOI nFinFET combining rotated substrate and strain. , 2016, , .		0
122	Influence of spacer materials on underlapped and self-aligned UTBB SOI nMOSFET. , 2016, , .		0
123	Understanding and optimizing the floating body retention in FDSOI UTBOX. Solid-State Electronics, 2016, 117, 123-129.	0.8	4
124	Low-Frequency Noise Analysis and Modeling in Vertical Tunnel FETs With Ge Source. IEEE Transactions on Electron Devices, 2016, 63, 1658-1665.	1.6	69
125	Performance of TFET and FinFET devices applied to current mirrors for different dimensions and temperatures. Semiconductor Science and Technology, 2016, 31, 055001.	1.0	10
126	Impact of Gate Stack Layer Composition on Dynamic Threshold Voltage and Analog Parameters of Ge pMOSFETs. Journal of Integrated Circuits and Systems, 2016, 11, 7-12.	0.3	0

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127	Analog performance of vertical nanowire TFETs as a function of temperature and transport mechanism. Solid-State Electronics, 2015, 112, 51-55.	0.8	17
128	The Impact of the Ge Concentration in the Source for Vertical Tunnel-FETs. ECS Transactions, 2015, 66, 79-86.	0.3	1
129	Enhanced dynamic threshold voltage UTBB SOI nMOSFETs. Solid-State Electronics, 2015, 112, 19-23.	0.8	10
130	High temperature influence on analog parameters of Bulk and SOI nFinFETs. , 2015, , .		1
131	Extensionless UTBB FDSOI Devices in Enhanced Dynamic Threshold Mode under Low Power Point of View. Journal of Low Power Electronics and Applications, 2015, 5, 69-80.	1.3	3
132	Threshold Voltage Modeling for Dynamic Threshold UTBB SOI in Different Operation Modes. ECS Transactions, 2015, 66, 109-115.	0.3	3
133	Study of Hysteresis in Vertical Ge-Source Heterojunction Tunnel-FETs at Low Temperature. ECS Transactions, 2015, 66, 179-185.	0.3	0
134	Vertical Nanowire TFET Diameter Influence on Intrinsic Voltage Gain for Different Inversion Conditions. ECS Transactions, 2015, 66, 187-192.	0.3	2
135	Proton Radiation Effects on the Analog Performance of Bulk n- and p-FinFETs. ECS Transactions, 2015, 66, 295-301.	0.3	3
136	Comparison of Current Mirrors Designed with TFET or FinFET Devices for Different Dimensions and Temperatures. ECS Transactions, 2015, 66, 303-308.	0.3	2
137	Impact of Gate Stack Dielectric on Intrinsic Voltage Gain and Low Frequency Noise in Ge pMOSFETs. ECS Transactions, 2015, 66, 309-314.	0.3	1
138	Enhanced dynamic threshold UTBB SOI at high temperature. , 2015, , .		4
139	Transconductance hump in vertical gate-all-around tunnel-FETs. , 2015, , .		0
140	Impact of supercoupling effect on mobility enhancement in UTBB SOI in dynamic threshold mode. , 2015, , .		0
141	Ground Plane influence on UTBB SOI nMOSFET analog parameters. , 2015, , .		2
142	Dynamic threshold voltage influence on Ge pMOSFET hysteresis. , 2015, , .		0
143	Reliability of film thickness extraction through CV curves of SOI p-i-n gated diodes. , 2015, , .		0
144	Performance comparison between TFET and FinFET differential pair. , 2015, , .		4

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145	Detailed analysis of transport properties of FinFETs through Y-Function method: Effects of substrate orientation and strain. , 2015, , .		1
146	Impact of diameter on TFET conduction mechanisms. , 2015, , .		1
147	Analysis of analog parameters in NW-TFETs with Si and SiGe source composition at high temperatures. , 2015, , .		5
148	Towards singleâ€trap spectroscopy: Generationâ€recombination noise in UTBOX SOI nMOSFETs. Physica Status Solidi C: Current Topics in Solid State Physics, 2015, 12, 292-298.	0.8	15
149	Study of low frequency noise in vertical NW-Tunnel FETs with different source compositions. , 2015, , .		2
150	Low-frequency noise investigation of n-channel 3D devices. Microelectronic Engineering, 2015, 147, 122-125.	1.1	2
151	In-depth low frequency noise evaluation of substrate rotation and strain engineering in n-type triple gate SOI FinFETs. Microelectronic Engineering, 2015, 147, 92-95.	1.1	2
152	Comparison between vertical silicon NW-TFET and NW-MOSFETfrom analog point of view. , 2015, , .		4
153	TCAD Strain Calibration Versus Nanobeam Diffraction of Source/Drain Stressors for Ge MOSFETs. IEEE Transactions on Electron Devices, 2015, 62, 1079-1084.	1.6	8
154	The smaller the noisier? Low frequency noise diagnostics of advanced semiconductor devices. , 2015, , .		2
155	Back Enhanced (BE) SOI pMOSFET. , 2015, , .		20
156	Impact of the diameter of vertical nanowire-tunnel FETs with Si and SiGe source composition on analog parameters. , 2015, , .		3
157	Influence of the Source Composition on the Analog Performance Parameters of Vertical Nanowire-TFETs. IEEE Transactions on Electron Devices, 2015, 62, 16-22.	1.6	29
158	Different stress techniques and their efficiency on triple-gate SOI n-MOSFETs. Solid-State Electronics, 2015, 103, 209-215.	0.8	3
159	Proposal of a process design methodology of Fully depleted SOI nMOSFET using only three photolithograph steps for educational application. , 2014, , .		2
160	Field effect transistors: From mosfet to Tunnel-Fet analog performance perspective. , 2014, , .		5
161	Influence of underlap on UTBB SOI MOSFETs in dynamic threshold mode. , 2014, , .		3
162	Drain induced barrier thinning on TFETs with different source/drain engineering. , 2014, , .		14

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163	(Invited) The Impact of a (Si)Ge Heterojunction on the Analog Performance of Vertical Tunnel FETs. ECS Transactions, 2014, 64, 127-133.	0.3	1
164	Unity gain frequency on FinFET and TFET devices. , 2014, , .		3
165	Comparison of analog performance between SOI and Bulk pFinFET. , 2014, , .		1
166	Influence of high temperature on substrate effect of UTBB SOI nMOSFETs. , 2014, , .		2
167	Floating body effect on n-channel bulk FinFETs for memory application. , 2014, , .		1
168	Ground plane influence on enhanced dynamic threshold UTBB SOI nMOSFETs. , 2014, , .		6
169	Silicon film thickness influence on enhanced dynamic threshold UTBB SOI nMOSFETs. , 2014, , .		2
170	Investigation of Bulk and DTMOS triple-gate devices under 60 MeV proton irradiation. Microelectronics Reliability, 2014, 54, 2349-2354.	0.9	2
171	Graphene for advanced devices applications. , 2014, , .		0
172	Analog performance of standard and uniaxial strained triple-gate SOI FinFETs under x-ray radiation. Semiconductor Science and Technology, 2014, 29, 125015.	1.0	2
173	The effect of X-Ray radiation dose rate on Triple-Gate SOI FinFETs parameters. , 2014, , .		1
174	The effect of X-Ray radiation on DIBL for standard and strained triple-gate SOI MuGFETs. , 2014, , .		0
175	Advantages of different source/drain engineering on scaled UTBOX FDSOI nMOSFETs at high temperature operation. Solid-State Electronics, 2014, 91, 53-58.	0.8	2
176	Threshold voltage extraction in Tunnel FETs. Solid-State Electronics, 2014, 93, 49-55.	0.8	28
177	Comparison between experimental and simulated strain profiles in Ge channels with embedded source/drain stressors. Physica Status Solidi C: Current Topics in Solid State Physics, 2014, 11, 1578-1582.	0.8	5
178	Spike Anneal Peak Temperature Impact on 1T-DRAM Retention Time. IEEE Electron Device Letters, 2014, 35, 639-641.	2.2	4
179	Low-frequency noise assessment in advanced UTBOX SOI nMOSFETs with different gate dielectrics. Solid-State Electronics, 2014, 97, 14-22.	0.8	28
180	Improved retention times in UTBOX nMOSFETs for 1T-DRAM applications. Solid-State Electronics, 2014, 97, 30-37.	0.8	8

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181	Fin width influence on analog performance of SOI and bulk FINFETs. , 2014, , .		5
182	Early voltage and intrinsic voltage gain in vertical nanowire-TFETs as a function of temperature. , 2014, , .		0
183	Parasitic Conduction Response to X-ray Radiation in Unstrained and Strained Triple-Gate SOI MuGFETs. Journal of Integrated Circuits and Systems, 2014, 9, 97-102.	0.3	0
184	Observation of the Two-Sided Read Window on UTBOX SOI 1T-DRAM: Measurement Setup, Numerical and Empirical Results. Journal of Integrated Circuits and Systems, 2014, 9, 91-96.	0.3	0
185	Experimental Comparison Between Trigate p-TFET and p-FinFET Analog Performance as a Function of Temperature. IEEE Transactions on Electron Devices, 2013, 60, 2493-2497.	1.6	60
186	Fully electron-beam-lithography SOI FinFET. , 2013, , .		1
187	Temperature dependence of LF noise in UTBB nMOSFETs. , 2013, , .		0
188	Two-sided read window observed on UTBOX SOI 1T-DRAM. , 2013, , .		0
189	Semiconductor film band gap influence on retention time of UTBOX SOI 1T-DRAM using pulsed back gate bias. , 2013, , .		2
190	Potential and limitations of UTBB SOI for advanced CMOS technologies. , 2013, , .		5
191	On the Variability of the Front-/Back-Channel LF Noise in UTBOX SOI nMOSFETs. IEEE Transactions on Electron Devices, 2013, 60, 444-450.	1.6	20
192	Low-frequency noise of n-type triple gate FinFETs fabricated on standard and 45Â° rotated substrates. Solid-State Electronics, 2013, 90, 121-126.	0.8	4
193	Optimizing the front and back biases for the best sense margin and retention time in UTBOX FBRAM. Solid-State Electronics, 2013, 90, 149-154.	0.8	25
194	Influence of substrate rotation on the low frequency noise of strained triple-gate MuGFETs. , 2013, , .		0
195	RTN assessment of traps in polysilicon cylindrical vertical FETs for NVM application. Microelectronic Engineering, 2013, 109, 105-108.	1.1	10
196	Stress engineering and proton radiation influence on off-state leakage current in triple-gate SOI devices. Solid-State Electronics, 2013, 90, 155-159.	0.8	2
197	Back bias influence on analog performance of pTFET. , 2013, , .		2
198	NW-TFET analog performance for different Ge source compositions. , 2013, , .		11

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199	The activation energy dependence on the electric field in UTBOX SOI FBRAM devices. , 2013, , .		0
200	(Invited) Transistor-Based Extraction of Carrier Lifetime and Interface Traps Densities in Silicon-on-Insulator Materials. ECS Transactions, 2013, 50, 225-236.	0.3	6
201	Enhancement of SOI Photodiode Sensitivity by Aluminum Grating. ECS Transactions, 2013, 53, 127-130.	0.3	4
202	Comparative Experimental Study between Tensile and Compressive Uniaxially Stressed nMuGFETs under X-ray Radiation Focusing on Analog Behavior. ECS Transactions, 2013, 53, 177-185.	0.3	0
203	Fin Dimension Influence on Mechanical Stressors in Triple-Gate SOI nMOSFETs. ECS Transactions, 2013, 53, 187-192.	0.3	0
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