# Joao Martino

List of Publications by Year
in descending order



| 406 | 1,947 | 394286 19 | 454834 30 |
|---|---|---|---|
| papers | citations | h-index | g-index |

| 407 | 407 | 407 | 920 |
|---|---|---|---|
| all docs | docs citations | times ranked | citing authors |

| # | Article | IF | Citations |
|---|---|---|---|
| 1 | Low-Frequency Noise Analysis and Modeling in Vertical Tunnel FETs With Ge Source. IEEE Transactions on Electron Devices, 2016, 63, 1658-1665. | 1.6 | 69 |
| 2 | Temperature impact on the tunnel fet off-state current components. Solid-State Electronics, 2012, 78, 141-146. | 0.8 | 68 |
| 3 | Analog performance and application of graded-channel fully depleted SOI MOSFETs. Solid-State Electronics, 2000, 44, 1219-1222. | 0.8 | 67 |
| 4 | Experimental Comparison Between Trigate p-TFET and p-FinFET Analog Performance as a Function of Temperature. IEEE Transactions on Electron Devices, 2013, 60, 2493-2497. | 1.6 | 60 |
| 5 | Graded-channel fully depleted Silicon-On-Insulator nMOSFET for reducing the parasitic bipolar effects. Solid-State Electronics, 2000, 44, 917-922. | 0.8 | 56 |
| 6 | InGaAs tunnel FET with sub-nanometer EOT and sub-60â€‰mV/dec sub-threshold swing at room temperature. Applied Physics Letters, 2016, 109, . | 1.5 | 48 |
| 7 | Analog circuit design using graded-channel silicon-on-insulator nMOSFETs. Solid-State Electronics, 2002, 46, 1215-1225. | 0.8 | 33 |
| 8 | An Asymmetric Channel SOI nMOSFET for Reducing Parasitic Effects and Improving Output Characteristics. Electrochemical and Solid-State Letters, 1999, 3, 50. | 2.2 | 32 |
| 9 | Advantages of the Graded-Channel SOI FD MOSFET for Application as a Quasi-Linear Resistor. IEEE Transactions on Electron Devices, 2005, 52, 967-972. | 1.6 | 32 |
| 10 | Evaluation of triple-gate FinFETs with SiO2â€“HfO2â€“TiN gate stack under analog operation. Solid-State Electronics, 2007, 51, 285-291. | 0.8 | 32 |
| 11 | Influence of the Source Composition on the Analog Performance Parameters of Vertical Nanowire-TFETs. IEEE Transactions on Electron Devices, 2015, 62, 16-22. | 1.6 | 29 |
| 12 | Study of line-TFET analog performance comparing with other TFET and MOSFET architectures. Solid-State Electronics, 2017, 128, 43-47. | 0.8 | 29 |
| 13 | Threshold voltage extraction in Tunnel FETs. Solid-State Electronics, 2014, 93, 49-55. | 0.8 | 28 |
| 14 | Low-frequency noise assessment in advanced UTBOX SOI nMOSFETs with different gate dielectrics. Solid-State Electronics, 2014, 97, 14-22. | 0.8 | 28 |
| 15 | Trapezoidal Cross-Sectional Influence on FinFET Threshold Voltage and Corner Effects. Journal of the Electrochemical Society, 2008, 155, H213. | 1.3 | 25 |
| 16 | Behavior of triple-gate Bulk FinFETs with and without DTMOS operation. Solid-State Electronics, 2012, 71, 63-68. | 0.8 | 25 |
| 17 | Optimizing the front and back biases for the best sense margin and retention time in UTBOX FBRAM. Solid-State Electronics, 2013, 90, 149-154. | 0.8 | 25 |
| 18 | The Dependence of Retention Time on Gate Length in UTBOX FBRAM With Different Source/Drain Junction Engineering. IEEE Electron Device Letters, 2012, 33, 940-942. | 2.2 | 24 |

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| 19 | Harmonic Distortion of Unstrained and Strained FinFETs Operating in Saturation. IEEE Transactions on Electron Devices, 2010, 57, 3303-3311. | 1.6 | 23 |
| 20 | Cryogenic operation of FinFETs aiming at analog applications. Cryogenics, 2009, 49, 590-594. | 0.9 | 21 |
| 21 | The temperature mobility degradation influence on the zero temperature coefficient of partially and fully depleted SOI MOSFETs. Microelectronics Journal, 2006, 37, 952-957. | 1.1 | 20 |
| 22 | On the Variability of the Front-/Back-Channel LF Noise in UTBOX SOI nMOSFETs. IEEE Transactions on Electron Devices, 2013, 60, 444-450. | 1.6 | 20 |
| 23 | Back Enhanced (BE) SOI pMOSFET. , 2015, , . | | 20 |
| 24 | Analog Figures of Merit of Vertically Stacked Silicon Nanosheets nMOSFETs With Two Different Metal Gates for the Sub-7 nm Technology Node Operating at High Temperatures. IEEE Transactions on Electron Devices, 2021, 68, 3630-3635. | 1.6 | 18 |
| 25 | Analog performance of vertical nanowire TFETs as a function of temperature and transport mechanism. Solid-State Electronics, 2015, 112, 51-55. | 0.8 | 17 |
| 26 | Model for the potential drop in the silicon substrate for thin-film SOI MOSFETs. Electronics Letters, 1990, 26, 1462. | 0.5 | 17 |
| 27 | Reconfigurable back enhanced (BE) SOI MOSFET used to build a logic inverter. , 2017, , . | | 16 |
| 28 | Towards singleâ€trap spectroscopy: Generationâ€recombination noise in UTBOX SOI nMOSFETs. Physica Status Solidi C: Current Topics in Solid State Physics, 2015, 12, 292-298. | 0.8 | 15 |
| 29 | Substrate influences on fully depleted enhancement mode SOI MOSFETs at room temperature and at 77 K. Solid-State Electronics, 1997, 41, 111-119. | 0.8 | 14 |
| 30 | High performance analog operation of double gate transistors with the graded-channel architecture at low temperatures. Solid-State Electronics, 2005, 49, 1569-1575. | 0.8 | 14 |
| 31 | Analog performance of standard and strained triple-gate silicon-on-insulator nFinFETs. Solid-State Electronics, 2008, 52, 1904-1909. | 0.8 | 14 |
| 32 | Low-Frequency Noise Studies on Fully Depleted UTBOX Silicon-on-Insulator nMOSFETs: Challenges and Opportunities. ECS Journal of Solid State Science and Technology, 2013, 2, Q205-Q210. | 0.9 | 14 |
| 33 | Drain induced barrier thinning on TFETs with different source/drain engineering. , 2014, , . | | 14 |
| 34 | Double Gate Tunnel-FET Working Like a Permittivity Based Biosensor with Different Drain to Gate and Drain to Biomaterial Alignments. ECS Journal of Solid State Science and Technology, 2019, 8, Q50-Q53. | 0.9 | 13 |
| 35 | Gain improvement in operational transconductance amplifiers using Graded-Channel SOI nMOSFETS. Microelectronics Journal, 2006, 37, 31-37. | 1.1 | 12 |
| 36 | The low-frequency noise behaviour of graded-channel SOI nMOSFETs. Solid-State Electronics, 2007, 51, 260-267. | 0.8 | 12 |

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| 37 | Threshold voltages of SOI MuGFETs. Solid-State Electronics, 2008, 52, 1877-1883. | 0.8 | 12 |
| 38 | Comparison of the Low-Frequency Noise of Bulk Triple-Gate FinFETs With and Without Dynamic Threshold Operation. IEEE Electron Device Letters, 2011, 32, 1597-1599. | 2.2 | 12 |
| 39 | Back Enhanced (BE) SOI MOSFET under non-conventional bias conditions. , 2017, , . | | 12 |
| 40 | Extraction of the oxide charges at the silicon substrate interface in Silicon-On-Insulator MOSFET's. Solid-State Electronics, 1999, 43, 2039-2046. | 0.8 | 11 |
| 41 | The impact of gate length scaling on UTBOX FDSOI devices: The digital/analog performance of extension-less structures. , 2012, , . | | 11 |
| 42 | Influence of 60-MeV Proton-Irradiation on Standard and Strained n- and p-Channel MuGFETs. IEEE Transactions on Nuclear Science, 2012, 59, 707-713. | 1.2 | 11 |
| 43 | NW-TFET analog performance for different Ge source compositions. , 2013, , . | | 11 |
| 44 | Analog design with Line-TFET device experimental data: from device to circuit level. Semiconductor Science and Technology, 2020, 35, 055025. | 1.0 | 11 |
| 45 | SOI technology characterization using SOI-MOS capacitor. Solid-State Electronics, 2005, 49, 109-116. | 0.8 | 10 |
| 46 | Evaluation of graded-channel SOI MOSFET operation at high temperatures. Microelectronics Journal, 2006, 37, 601-607. | 1.1 | 10 |
| 47 | Modeling Silicon on Insulator MOS Transistors with Nonrectangular-Gate Layouts. Journal of the Electrochemical Society, 2006, 153, G218. | 1.3 | 10 |
| 48 | Low-frequency noise and static analysis of the impact of the TiN metal gate thicknesses on n- and p-channel MuGFETs. Solid-State Electronics, 2010, 54, 1592-1597. | 0.8 | 10 |
| 49 | Temperature influence on UTBOX 1T-DRAM using GIDL for writing operation. , 2012, , . | | 10 |
| 50 | RTN assessment of traps in polysilicon cylindrical vertical FETs for NVM application. Microelectronic Engineering, 2013, 109, 105-108. | 1.1 | 10 |
| 51 | Enhanced dynamic threshold voltage UTBB SOI nMOSFETs. Solid-State Electronics, 2015, 112, 19-23. | 0.8 | 10 |
| 52 | Impact of the NW-TFET Diameter on the Efficiency and the Intrinsic Voltage Gain From a Conduction Regime Perspective. IEEE Transactions on Electron Devices, 2016, 63, 2930-2935. | 1.6 | 10 |
| 53 | Performance of TFET and FinFET devices applied to current mirrors for different dimensions and temperatures. Semiconductor Science and Technology, 2016, 31, 055001. | 1.0 | 10 |
| 54 | Parameter Extraction of MOSFETs Operated at Low Temperature. European Physical Journal Special Topics, 1996, 06, C3-29-C3-42. | 0.2 | 9 |

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| 55 | Study of the linear kink effect in PD SOI nMOSFETs. Microelectronics Journal, 2007, 38, 114-119. | 1.1 | 9 |
| 56 | Trapezoidal SOI FinFET analog parameters' dependence on cross-section shape. Semiconductor Science and Technology, 2009, 24, 115017. | 1.0 | 9 |
| 57 | Zero Temperature Coefficient behavior for advanced MOSFETs. , 2016, , . | | 9 |
| 58 | Intrinsic voltage gain of Line-TFETs and comparison with other TFET and MOSFET architectures. , 2016, , . | | 9 |
| 59 | GR-Noise Characterization of Ge pFinFETs With STI First and STI Last Processes. IEEE Electron Device Letters, 2016, 37, 1092-1095. | 2.2 | 9 |
| 60 | Performance evaluation of Tunnel-FET basic amplifier circuits. , 2019, , . | | 9 |
| 61 | Low frequency noise performance of horizontal, stacked and vertical silicon nanowire MOSFETs. Solid-State Electronics, 2021, 184, 108087. | 0.8 | 9 |
| 62 | Investigation of back gate interface states by drain current hysteresis in PD-SOI n-MOSFETs. Physica B: Condensed Matter, 2006, 376-377, 416-419. | 1.3 | 8 |
| 63 | Electron valence-band tunnelling excess noise in twin-gate silicon-on-insulator MOSFETs. Solid-State Electronics, 2006, 50, 52-57. | 0.8 | 8 |
| 64 | Fin shape influence on the analog performance of standard and strained MuGFETs. , 2010, , . | | 8 |
| 65 | Substrate effect on UTBB SOI nMOSFET. , 2013, , . | | 8 |
| 66 | Improved retention times in UTBOX nMOSFETs for 1T-DRAM applications. Solid-State Electronics, 2014, 97, 30-37. | 0.8 | 8 |
| 67 | TCAD Strain Calibration Versus Nanobeam Diffraction of Source/Drain Stressors for Ge MOSFETs. IEEE Transactions on Electron Devices, 2015, 62, 1079-1084. | 1.6 | 8 |
| 68 | Back gate bias influence on SOI Î©-gate nanowire down to 10 nm width. , 2016, , . | | 8 |
| 69 | Low-Frequency Noise Assessment of Different Ge pFinFET STI Processes. IEEE Transactions on Electron Devices, 2016, 63, 4031-4037. | 1.6 | 8 |
| 70 | Optimization of the permittivity-based BE SOI biosensor. , 2018, , . | | 8 |
| 71 | Operational transconductance amplifier designed with nanowire tunnel-FET with Si, SiGe and Ge sources using experimental data. Semiconductor Science and Technology, 2020, 35, 095020. | 1.0 | 8 |
| 72 | Simple method for the determination of the interface trap density at 77 K in fully depleted accumulation mode SOI MOSFETs. Solid-State Electronics, 1993, 36, 827-832. | 0.8 | 7 |

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| 73 | Transient effects in accumulation mode p-channel SOI MOSFET's operating at 77 K. IEEE Transactions on Electron Devices, 1994, 41, 519-523. | 1.6 | 7 |
| 74 | A new method for determining the front and back interface trap densities of accumulation mode SOI MOSFETs at 77K. Solid-State Electronics, 1995, 38, 1799-1803. | 0.8 | 7 |
| 75 | Estimating Temperature Dependence of Generation Lifetime Extracted from Drain Current Transients. Journal of the Electrochemical Society, 2006, 153, G502. | 1.3 | 7 |
| 76 | Zero-Temperature-Coefficient of planar and MuGFET SOI devices. , 2010, , . | | 7 |
| 77 | Comparative analysis of the intrinsic voltage gain and unit gain frequency between SOI and bulk FinFETs up to high temperatures. Solid-State Electronics, 2016, 123, 124-129. | 0.8 | 7 |
| 78 | Optimization of the silicon thickness on Back Enhanced (BE) SOI pMOSFET working as a visible spectrum light sensor. , 2018, , . | | 7 |
| 79 | Back Enhanced SOI MOSFET as UV Light Sensor. , 2018, , . | | 7 |
| 80 | Impact of Biosensor Permittivity on a Double-Gate nTFET Ambipolar Current. ECS Transactions, 2018, 85, 187-192. | 0.3 | 7 |
| 81 | Tradeoff between the transistor reconfigurable technology and the zero-temperature-coefficient (ZTC) bias point on BESOI MOSFET. Microelectronics Journal, 2019, 94, 104658. | 1.1 | 7 |
| 82 | Study of <sup>Î'Î•</sup>SOI MOSFET Reconfigurable Transistor for Biosensing Application. ECS Journal of Solid State Science and Technology, 2021, 10, 027004. | 0.9 | 7 |
| 83 | Early Voltage Behavior in Circular Gate SOI nMOSFET Using 0.13 Î¼m Partially-Depleted SOI CMOS Technology. ECS Transactions, 2007, 4, 309-318. | 0.3 | 6 |
| 84 | GIDL behavior of p- and n-MuGFET devices with different TiN metal gate thickness and high-k gate dielectrics. Solid-State Electronics, 2012, 70, 44-49. | 0.8 | 6 |
| 85 | (Invited) Transistor-Based Extraction of Carrier Lifetime and Interface Traps Densities in Silicon-on-Insulator Materials. ECS Transactions, 2013, 50, 225-236. | 0.3 | 6 |
| 86 | Lessons Learned from Low-Frequency Noise Studies on Fully Depleted UTBOX Silicon-On-Insulator nMOSFETs. ECS Transactions, 2013, 53, 49-61. | 0.3 | 6 |
| 87 | Ground plane influence on enhanced dynamic threshold UTBB SOI nMOSFETs. , 2014, , . | | 6 |
| 88 | Analysis of current mirror circuits designed with line tunnel FET devices at different temperatures. Semiconductor Science and Technology, 2017, 32, 055015. | 1.0 | 6 |
| 89 | Influence of biological element permittivity on BE (Back Enhanced) SOI MOSFETs. , 2018, , . | | 6 |
| 90 | Optimization of Source/Drain Schottky Barrier Height on BE SOI MOSFET. ECS Transactions, 2018, 85, 79-84. | 0.3 | 6 |

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| 91 | Analytical modeling of the substrate influences on accumulation-mode SOI pMOSFETs at room temperature and at liquid nitrogen temperature. Solid-State Electronics, 1997, 41, 1241-1246. | 0.8 | 5 |
| 92 | Analysis of transition region and accumulation layer effect in the subthreshold slope in SOI nMOSFETs and their influences on the interface trap density extraction. Solid-State Electronics, 1999, 43, 2191-2199. | 0.8 | 5 |
| 93 | Extraction of the lightly doped drain concentration of fully depleted SOI NMOSFETs using the back gate bias effect. Solid-State Electronics, 2000, 44, 677-684. | 0.8 | 5 |
| 94 | A physically-based continuous analytical graded-channel SOI nMOSFET model for analog applications. , 0, , . | | 5 |
| 95 | Impact of halo implantation on 0.13Î¼m floating body partially depleted SOI n-MOSFETs in low temperature operation. Solid-State Electronics, 2005, 49, 1274-1281. | 0.8 | 5 |
| 96 | Analysis of Temperature-Induced Saturation Threshold Voltage Degradation in Deep-Submicrometer Ultrathin SOI MOSFETs. IEEE Transactions on Electron Devices, 2005, 52, 2236-2242. | 1.6 | 5 |
| 97 | Impact of the twin-gate structure on the linear kink effect in PD SOI nMOSFETS. Microelectronics Journal, 2006, 37, 681-685. | 1.1 | 5 |
| 98 | Improved generation lifetime model for the electrical characterization of single- and double-gate SOI nMOSFETs. Semiconductor Science and Technology, 2008, 23, 125011. | 1.0 | 5 |
| 99 | Analog Performance of Gate-Source/Drain Underlap Triple-Gate SOI nMOSFET. ECS Transactions, 2011, 39, 239-246. | 0.3 | 5 |
| 100 | The impact of back bias on the floating body effect in UTBOX SOI devices for 1T-FBRAM memory applications. , 2012, , . | | 5 |
| 101 | Potential and limitations of UTBB SOI for advanced CMOS technologies. , 2013, , . | | 5 |
| 102 | Field effect transistors: From mosfet to Tunnel-Fet analog performance perspective. , 2014, , . | | 5 |
| 103 | Comparison between experimental and simulated strain profiles in Ge channels with embedded source/drain stressors. Physica Status Solidi C: Current Topics in Solid State Physics, 2014, 11, 1578-1582. | 0.8 | 5 |
| 104 | Fin width influence on analog performance of SOI and bulk FINFETs. , 2014, , . | | 5 |
| 105 | Analysis of analog parameters in NW-TFETs with Si and SiGe source composition at high temperatures. , 2015, , . | | 5 |
| 106 | Analog parameters of solid source Zn diffusion In<sub>X</sub>Ga<sub>1â^'X</sub>As nTFETs down to 10 K. Semiconductor Science and Technology, 2016, 31, 124001. | 1.0 | 5 |
| 107 | Back enhanced (BE) SOI pMOSFET behavior at high temperatures. , 2016, , . | | 5 |
| 108 | Is there a Zero Temperature bias point (ZTC) on Back Enhanced (BE) SOI MOSFET?. , 2017, , . | | 5 |

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| 109 | Performance of differential pair circuits designed with line tunnel FET devices at different temperatures. Semiconductor Science and Technology, 2018, 33, 075012. | 1.0 | 5 |
| 110 | One Transistor Floating Body RAM Performances on UTBOX Devices Using the BJT Effect. Journal of Integrated Circuits and Systems, 2012, 7, 113-120. | 0.3 | 5 |
| 111 | Influence of accumulation layer on interface trap density extraction. Electronics Letters, 1998, 34, 2439. | 0.5 | 4 |
| 112 | Simultaneous extraction of the silicon film and front oxide thicknesses on fully depleted SOI nMOSFETs. Solid-State Electronics, 2000, 44, 1961-1969. | 0.8 | 4 |
| 113 | Cryogenic operation of graded-channel silicon-on-insulator nMOSFETs for high performance analog applications. Microelectronics Journal, 2006, 37, 137-144. | 1.1 | 4 |
| 114 | Impact of Asymmetric Channel Configuration on the Linearity of Double-Gate SOI MOSFETs. , 2006, , . | | 4 |
| 115 | Transconductance ramp effect in high-k triple gate sSOI nFinFETs. , 2009, , . | | 4 |
| 116 | Improved Analytical Model for ZTC Bias Point for Strained Tri-gates FinFETs. ECS Transactions, 2010, 31, 385-392. | 0.3 | 4 |
| 117 | Influence of the sidewall crystal orientation, HfSiO nitridation and TiN metal gate thickness on n-MuGFETs under analog operation. Solid-State Electronics, 2011, 62, 146-151. | 0.8 | 4 |
| 118 | Temperature Influence on Tunnel Field Effect Transistors (TFETs) with Low Ambipolar Currents. ECS Transactions, 2011, 39, 77-84. | 0.3 | 4 |
| 119 | Comparison between low and high read bias in FB-RAM on UTBOX FDSOI devices. , 2012, , . | | 4 |
| 120 | Analysis of temperature variation influence on the analog performance of 45Â° rotated triple-gate nMuGFETs. Solid-State Electronics, 2012, 70, 39-43. | 0.8 | 4 |
| 121 | Low-frequency noise of n-type triple gate FinFETs fabricated on standard and 45Â° rotated substrates. Solid-State Electronics, 2013, 90, 121-126. | 0.8 | 4 |
| 122 | Enhancement of SOI Photodiode Sensitivity by Aluminum Grating. ECS Transactions, 2013, 53, 127-130. | 0.3 | 4 |
| 123 | Spike Anneal Peak Temperature Impact on 1T-DRAM Retention Time. IEEE Electron Device Letters, 2014, 35, 639-641. | 2.2 | 4 |
| 124 | Enhanced dynamic threshold UTBB SOI at high temperature. , 2015, , . | | 4 |
| 125 | Performance comparison between TFET and FinFET differential pair. , 2015, , . | | 4 |
| 126 | Comparison between vertical silicon NW-TFET and NW-MOSFETfrom analog point of view. , 2015, , . | | 4 |

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| 127 | Effective hole mobility and low-frequency noise characterization of Ge pFinFETs. , 2016, , . | | 4 |
| 128 | Improved operation of graded-channel SOI nMOSFETs down to liquid helium temperature. Semiconductor Science and Technology, 2016, 31, 114005. | 1.0 | 4 |
| 129 | Understanding and optimizing the floating body retention in FDSOI UTBOX. Solid-State Electronics, 2016, 117, 123-129. | 0.8 | 4 |
| 130 | Experimental analysis of differential pairs designed with line tunnel FET devices. , 2017, , . | | 4 |
| 131 | A Tunnel-FET device model based on Verilog-A applied to circuit simulation. , 2018, , . | | 4 |
| 132 | Silicon Nanowire Tunnel-FET Differential Amplifier Using Verilog-A Lookup Table Approach. , 2019, , . | | 4 |
| 133 | Gate dielectric material influence on DC behavior of MO(I)SHEMT devices operating up to 150ÂÂ°C. Solid-State Electronics, 2021, 185, 108091. | 0.8 | 4 |
| 134 | Low temperature operation of graded-channel SOI nMOSFETs for analog applications. European Physical Journal Special Topics, 2002, 12, 23-26. | 0.2 | 4 |
| 135 | Fabrication and Electrical Characterization of Ultra-Thin Body and BOX (UTBB) Back Enhanced SOI (BESOI) pMOSFET. Journal of Integrated Circuits and Systems, 2020, 15, 1-6. | 0.3 | 4 |
| 136 | Fin Cross-Section Shape Influence on Short Channel Effects of MuGFETs. Journal of Integrated Circuits and Systems, 2012, 7, 137-144. | 0.3 | 4 |
| 137 | Analog circuit design using graded-channel SOI nMOSFETs. , 0, , . | | 3 |
| 138 | Physical and Electrical Characterization of Thin Nickel Films Obtained from Electroless Plating onto Aluminum. Physica Status Solidi A, 2001, 187, 75-84. | 1.7 | 3 |
| 139 | Analog Operation of Uniaxially Strained FD SOI nMOSFETs in Cryogenic Temperatures. SOI Conference, Proceedings of the IEEE International, 2007, , . | 0.0 | 3 |
| 140 | Temperature Influences on FinFETs with Undoped Body. ECS Transactions, 2007, 6, 211-216. | 0.3 | 3 |
| 141 | Low temperature influence on the uniaxially strained FD SOI nMOSFETs behavior. Microelectronic Engineering, 2007, 84, 2121-2124. | 1.1 | 3 |
| 142 | DIBL Study Using Triple Gate Unstrained and Uniaxial/Biaxial Strained FinFETs. ECS Transactions, 2009, 23, 591-596. | 0.3 | 3 |
| 143 | Analog Performance of Bulk and DTMOS Triple-Gate Devices. ECS Transactions, 2010, 31, 67-74. | 0.3 | 3 |
| 144 | Impact of proton irradiation on strained triple gate SOI p- and n-MOSFETs. , 2011, , . | | 3 |

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| 145 | Behavior of triple gate Bulk FinFETs with and without DTMOS operation. , 2011, , . | | 3 |
| 146 | Harmonic distortion of 2-MOS structures for MOSFET-C filters implemented with n-type unstrained and strained FINFETS. Solid-State Electronics, 2011, 62, 99-105. | 0.8 | 3 |
| 147 | Analysis of UTBOX 1T-DRAM Memory Cell at High Temperatures. ECS Transactions, 2011, 39, 61-68. | 0.3 | 3 |
| 148 | Analysis of the Silicon Film Thickness and the Ground Plane Influence on Ultra Thin Buried Oxide SOI nMOSFETs. ECS Transactions, 2012, 49, 511-517. | 0.3 | 3 |
| 149 | Experimental analog performance of pTFETs as a function of temperature. , 2012, , . | | 3 |
| 150 | An analytic method to compute the stress dependence on the dimensions and its influence in the characteristics of triple gate devices. Microelectronics Reliability, 2012, 52, 519-524. | 0.9 | 3 |
| 151 | Impact of Dynamic Body Floating effect on Low-Energy Operation of XCT-SOI CMOS Devices with Aim of Sub-20-nm Regime. ECS Transactions, 2013, 53, 75-84. | 0.3 | 3 |
| 152 | Temperature Influence on Strained nMuGFETs after Proton Radiation. ECS Transactions, 2013, 53, 171-176. | 0.3 | 3 |
| 153 | Experimental Comparison between pTFET and pFinFET under Analog Operation. ECS Transactions, 2013, 53, 155-160. | 0.3 | 3 |
| 154 | Influence of High Temperature on UTBB SOI nMOSFETs with and without Ground Plane. ECS Transactions, 2013, 53, 85-91. | 0.3 | 3 |
| 155 | Influence of underlap on UTBB SOI MOSFETs in dynamic threshold mode. , 2014, , . | | 3 |
| 156 | Unity gain frequency on FinFET and TFET devices. , 2014, , . | | 3 |
| 157 | Extensionless UTBB FDSOI Devices in Enhanced Dynamic Threshold Mode under Low Power Point of View. Journal of Low Power Electronics and Applications, 2015, 5, 69-80. | 1.3 | 3 |
| 158 | Threshold Voltage Modeling for Dynamic Threshold UTBB SOI in Different Operation Modes. ECS Transactions, 2015, 66, 109-115. | 0.3 | 3 |
| 159 | Proton Radiation Effects on the Analog Performance of Bulk n- and p-FinFETs. ECS Transactions, 2015, 66, 295-301. | 0.3 | 3 |
| 160 | Impact of the diameter of vertical nanowire-tunnel FETs with Si and SiGe source composition on analog parameters. , 2015, , . | | 3 |
| 161 | Different stress techniques and their efficiency on triple-gate SOI n-MOSFETs. Solid-State Electronics, 2015, 103, 209-215. | 0.8 | 3 |
| 162 | Low Temperature Effect on Strained and Relaxed Ge pFinFETs STI Last Processes. ECS Transactions, 2016, 75, 213-218. | 0.3 | 3 |

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| 163 | Ground plane influence on zero-temperature-coefficient in SOI UTBB MOSFETs with different silicon film thicknesses. , 2016, , . | | 3 |
| 164 | The Influence of Oxide Thickness and Indium Amount on the Analog Parameters of In<sub><italic>x</italic></sub>Ga<sub>1â€“<italic>x</italic></sub>As nTFETs. IEEE Transactions on Electron Devices, 2017, 64, 3595-3600. | 1.6 | 3 |
| 165 | Is there a kink effect in FDSOI MOSFETs?. , 2017, , . | | 3 |
| 166 | Proton radiation effects on the self-aligned triple gate SOI p-type tunnel FET output characteristic. , 2017, , . | | 3 |
| 167 | Third Generation BESOI (Back-Enhanced SOI) pMOSFET fabricated on UTBB Wafer. , 2019, , . | | 3 |
| 168 | Impact of Schottky contacts on p-type back enhanced SOI MOSFETs. Solid-State Electronics, 2020, 169, 107815. | 0.8 | 3 |
| 169 | Intrinsic Voltage Gain of Stacked GAA Nanosheet MOSFETs Operating at High Temperatures. ECS Transactions, 2020, 97, 65-69. | 0.3 | 3 |
| 170 | Gate Oxide Thickness Influence on the Gate Induced Floating Body Effect in SOI Technology. Journal of Integrated Circuits and Systems, 2008, 3, 91-95. | 0.3 | 3 |
| 171 | Investigation of the Gate Length and Drain Bias Dependence of the ZTC Biasing Point Instability of N- and P-Channel PD SOI MOSFETs. Journal of Integrated Circuits and Systems, 2009, 4, 61-66. | 0.3 | 3 |
| 172 | Impact of Selective Epitaxial Growth and Uniaxial/Biaxial Strain on DIBL Effect Using Triple Gate FinFETs. Journal of Integrated Circuits and Systems, 2010, 5, 154-159. | 0.3 | 3 |
| 173 | Analytical modeling of the substrate effect on accumulation-mode SOI pMOSFETs at room temperature and at 77 K. Microelectronic Engineering, 1997, 36, 375-378. | 1.1 | 2 |
| 174 | Extraction of the oxide charge density at front and back interfaces of SOI nMOSFETs devices. Solid-State Electronics, 2002, 46, 1381-1387. | 0.8 | 2 |
| 175 | Low Temperature and Channel Engineering Influence on Harmonic Distortion of SOI nMOSFETs for Analog Applications. ECS Meeting Abstracts, 2005, , . | 0.0 | 2 |
| 176 | Analysis of uniaxial and biaxial strain impact on the linearity of fully depleted SOI nMOSFETs. Solid-State Electronics, 2007, 51, 1194-1200. | 0.8 | 2 |
| 177 | Temperature influence on the gate-induced floating body effect parameters in fully depleted SOI nMOSFETs. Solid-State Electronics, 2008, 52, 1751-1754. | 0.8 | 2 |
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