Xiaowei Li

List of Publications by Year in descending order

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265 papers	2,724 citations	471371 17 h-index	477173 29 g-index
266 all docs	266 docs citations	266 times ranked	1819 citing authors

#	Article	IF	Citations
1	On-Line Fault Protection for ReRAM-Based Neural Networks. IEEE Transactions on Computers, 2023, 72, 423-437.	2.4	1
2	A Fast Precision Tuning Solution for Always-On DNN Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1236-1248.	1.9	1
3	Saving Energy of RRAM-Based Neural Accelerator Through State-Aware Computing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2115-2127.	1.9	0
4	VNet: a versatile network to train real-time semantic segmentation models on a single GPU. Science China Information Sciences, 2022, 65, 1.	2.7	2
5	An Efficient Deep Learning Accelerator Architecture for Compressed Video Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2808-2820.	1.9	1
6	HyCA: A Hybrid Computing Architecture for Fault-Tolerant Deep Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3400-3413.	1.9	10
7	Taming Process Variations in CNFET for Efficient Last-Level Cache Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 418-431.	2.1	0
8	SATAM: A SAT Attack Resistant Active Metering Against IC Overbuilding. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 2025-2041.	3.2	3
9	A Voltage Template Attack on the Modular Polynomial Subtraction in Kyber. , 2022, , .		3
10	DOE: Database Offloading Engine for Accelerating SQL Processing. , 2022, , .		1
11	HTDet: A clustering method using information entropy for hardware Trojan detection. Tsinghua Science and Technology, 2021, 26, 48-61.	4.1	20
12	An Edge 3D CNN Accelerator for Low-Power Activity Recognition. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 918-930.	1.9	10
13	To cloud or not to cloud: an on-line scheduler for dynamic privacy-protection of deep learning workload on edge devices. CCF Transactions on High Performance Computing, 2021, 3, 85-100.	1.1	3
14	EnGN: A High-Throughput and Energy-Efficient Accelerator for Large Graph Neural Networks. IEEE Transactions on Computers, 2021, 70, 1511-1525.	2.4	64
15	Chaotic Weights: A Novel Approach to Protect Intellectual Property of Deep Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1327-1339.	1.9	29
16	Happy Emotion Recognition From Unconstrained Videos Using 3D Hybrid Deep Features. IEEE Access, 2021, 9, 35524-35538.	2.6	14
17	CAP: Communication-aware Automated Parallelization for Deep Learning Inference on CMP Architectures. IEEE Transactions on Computers, 2021, , 1-1.	2.4	2
18	R2F: A Remote Retraining Framework for AIoT Processors With Computing Errors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1955-1966.	2.1	5

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19	Reliability Evaluation and Analysis of FPGA-Based Neural Network Acceleration System. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 472-484.	2.1	19
20	Adjustable and Configurable Ring Oscillator Physical Unclonable Function. Jisuanji Fuzhu Sheji Yu Tuxingxue Xuebao/Journal of Computer-Aided Design and Computer Graphics, 2021, 33, 340-345.	0.2	1
21	Special Session - Test for AI Chips: from DFT to On-line Testing. , 2021, , .		1
22	Internet connected vehicle platoon system modeling and linear stability analysis. Computer Communications, 2021, 174, 92-100.	3.1	12
23	Editorial for the special issue on reliability and power efficiency for HPC. CCF Transactions on High Performance Computing, 2021, 3, 1-3.	1.1	0
24	KFS-LIO: Key-Feature Selection for Lightweight Lidar Inertial Odometry. , 2021, , .		5
25	BitX: Empower Versatile Inference with Hardware Runtime Pruning. , 2021, , .		3
26	GCiM: A Near-Data Processing Accelerator for Graph Construction. , 2021, , .		3
27	PixelSieve: Towards Efficient Activity Analysis From Compressed Video Streams. , 2021, , .		0
28	TARe: Task-Adaptive in-situ ReRAM Computing for Graph Learning. , 2021, , .		4
29	SeGa: A Trojan Detection Method Combined With Gate Semantics. , 2021, , .		1
30	Software-Based Self-Testing Using Bounded Model Checking for Out-of-Order Superscalar Processors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 714-727.	1.9	9
31	GPGPU-Based ATPG System: Myth or Reality?. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 239-247.	1.9	2
32	Architecting Effectual Computation for Machine Learning Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2654-2667.	1.9	3
33	BZIP: A compact data memory system for UTXO-based blockchains. Journal of Systems Architecture, 2020, 109, 101809.	2.5	14
34	Exploring Spatial-Temporal Multi-Frequency Analysis for High-Fidelity and Temporal-Consistency Video Prediction. , 2020, , .		50
35	Persistent Fault Analysis of Neural Networks on FPGA-based Acceleration System. , 2020, , .		7
36	Evaluating and Constraining Hardware Assertions with Absent Scenarios. Journal of Computer Science and Technology, 2020, 35, 1198-1216.	0.9	1

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37	MultiPAD: A Multivariant Partition-Based Method for Audio Adversarial Examples Detection. IEEE Access, 2020, 8, 63368-63380.	2.6	7
38	A Guaranteed Secure Scan Design Based on Test Data Obfuscation by Cryptographic Hash. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4524-4536.	1.9	16
39	Sequence Triggered Hardware Trojan in Neural Network Accelerator. , 2020, , .		12
40	Trajectory Tracking Based on Adaptive Sliding Mode Control for Agricultural Tractor. IEEE Access, 2020, 8, 113021-113029.	2.6	15
41	Search-free Accelerator for Sparse Convolutional Neural Networks. , 2020, , .		2
42	Multi-Granularity Reconfiguration based Physical Unclonable Function Design. , 2020, , .		0
43	INORâ€"An Intelligent noise reduction method to defend against adversarial audio examples. Neurocomputing, 2020, 401, 160-172.	3.5	5
44	Prediction Stability: A New Metric for Quantitatively Evaluating DNN Outputs. , 2020, , .		0
45	CNT-Cache: an Energy-Efficient Carbon Nanotube Cache with Adaptive Encoding. , 2020, , .		1
46	Towards State-Aware Computation in ReRAM Neural Networks. , 2020, , .		4
47	An Efficient Deep Learning Accelerator for Compressed Video Analysis. , 2020, , .		3
48	A many-core accelerator design for on-chip deep reinforcement learning. , 2020, , .		5
49	DeepBurning-GL. , 2020, , .		17
50	Two-Stage Safe Reinforcement Learning for High-Speed Autonomous Racing. , 2020, , .		7
51	Survey: Hardware Trojan Detection for Netlist. , 2020, , .		13
52	Optimization Space Exploration of Hardware Design for CRYSTALS-KYBER. , 2020, , .		3
53	ShuttleNoC: Power-Adaptable Communication Infrastructure for Many-Core Processors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1438-1451.	1.9	3
54	BZIP: A Compact Data Memory System for UTXO-based Blockchains. , 2019, , .		7

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55	SqueezeFlow: A Sparse CNN Accelerator Exploiting Concise Convolution Rules. IEEE Transactions on Computers, 2019, 68, 1663-1677.	2.4	33
56	Learn-to-Scale: Parallelizing Deep Learning Inference on Chip Multiprocessor Architecture. , 2019, , .		7
57	Scan Chain Based Attacks and Countermeasures: A Survey. IEEE Access, 2019, 7, 85055-85065.	2.6	17
58	Squeezing the Last MHz for CNN Acceleration on FPGAs. , 2019, , .		8
59	Implementation of Parametric Hardware Trojan in FPGA. , 2019, , .		0
60	Instruction Vulnerability Test and Code Optimization Against DVFS Attack. , 2019, , .		1
61	Leveraging Memory PUFs and PIM-based encryption to secure edge deep learning systems. , 2019, , .		5
62	P ³ M. , 2019, , .		13
63	ShuntFlow. , 2019, , .		3
64	HeadStart. , 2019, , .		2
65	A None-Sparse Inference Accelerator that Distills and Reuses the Computation Redundancy in CNNs. , 2019, , .		7
66	Accelerating DNN-based 3D point cloud processing for mobile computing. Science China Information Sciences, 2019, 62, 1.	2.7	6
67	Resilient Neural Network Training for Accelerators with Computing Errors. , 2019, , .		12
68	TNPU. , 2019, , .		9
69	Redeeming chip-level power efficiency by collaborative management of the computation and communication. , 2019, , .		0
70	Exploring emerging CNFET for efficient last level cache design. , 2019, , .		3
71	Systolic Cube. , 2019, , .		12
72	Addressing the issue of processing element under-utilization in general-purpose systolic deep learning accelerators. , 2019, , .		16

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73	Simulate-the-hardware. , 2019, , .		4
74	An Agile Precision-Tunable CNN Accelerator based on ReRAM. , 2019, , .		9
75	Asian Test Symposium - Past, Present and Future -. , 2019, , .		0
76	Thread: Towards fine-grained precision reconfiguration in variable-precision neural network accelerator. IEICE Electronics Express, 2019, 16, 20190145-20190145.	0.3	3
77	China Test Conference (CTC) - Extending the Global Test Forum to China. , 2019, , .		0
78	MLA: Machine Learning Adaptation for Realtime Streaming Financial Applications. , 2019, , .		2
79	RRAMedy: Protecting ReRAM-Based Neural Network from Permanent and Soft Faults During Its Lifetime. , 2019, , .		16
80	When Deep Learning Meets the Edge: Auto-Masking Deep Neural Networks for Efficient Machine Learning on Edge Devices. , 2019, , .		2
81	VNet: A Versatile Network for Efficient Real-Time Semantic Segmentation. , 2019, , .		3
82	GramsDet: Hardware Trojan Detection Based on Recurrent Neural Network. , 2019, , .		13
83	InS-DLA: An In-SSD Deep Learning Accelerator for Near-Data Processing. , 2019, , .		11
84	Adjustable Arbiter Physical Unclonable Function with Flexible Response Distribution. , 2019, , .		1
85	iATPG: Instruction-level Automatic Test Program Generation for Vulnerabilities under DVFS attack. , 2019, , .		1
86	SynergyFlow. ACM Transactions on Design Automation of Electronic Systems, 2019, 24, 1-27.	1.9	5
87	Promoting the Harmony between Sparsity and Regularity: A Relaxed Synchronous Architecture for Convolutional Neural Networks. IEEE Transactions on Computers, 2019, 68, 867-881.	2.4	3
88	A QoS-QoR Aware CNN Accelerator Design Approach. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1995-2007.	1.9	3
89	PUFPass: A password management mechanism based on software/hardware codesign. The Integration VLSI Journal, 2019, 64, 173-183.	1.3	4
90	PIMSim: A Flexible and Detailed Processing-in-Memory Simulator. IEEE Computer Architecture Letters, 2019, 18, 6-9.	1.0	26

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91	Cluster Restoration-Based Trace Signal Selection for Post-Silicon Debug. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 767-779.	1.9	4
92	XORiM: A case of in-memory bit-comparator implementation and its performance implications. , 2018, , .		1
93	LMDet: A â€œNaturalnessâ€•Statistical Method for Hardware Trojan Detection. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 720-732.	2.1	11
94	Deterministic and Probabilistic Diagnostic Challenge Generation for Arbiter Physical Unclonable Function. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 3186-3197.	1.9	3
95	PIMCH: Cooperative memory prefetching in processing-in-memory architecture. , 2018, , .		5
96	A Case of On-Chip Memory Subsystem Design for Low-Power CNN Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1971-1984.	1.9	10
97	On Trace Buffer Reuse-Based Trigger Generation in Post-Silicon Debug. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2166-2179.	1.9	2
98	CCR: A concise convolution rule for sparse neural network accelerators. , 2018, , .		7
99	A Low Overhead In-Network Data Compressor for the Memory Hierarchy of Chip Multiprocessors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1265-1277.	1.9	7
100	AdaFlow: Aggressive Convolutional Neural Networks Approximation by Leveraging the Input Variability. Journal of Low Power Electronics, 2018, 14, 481-495.	0.6	0
101	Hardware Trojan Detection Based on Signal Correlation. , 2018, , .		7
102	Lightweight Timing Channel Protection for Shared DRAM Controller. , 2018, , .		1
103	Optimizing Memory Efficiency for Deep Convolutional Neural Network Accelerators. Journal of Low Power Electronics, 2018, 14, 496-507.	0.6	0
104	Hardware Trojan in FPGA CNN Accelerator. , 2018, , .		17
105	RiskCap: Minimizing Effort of Error Regulation for Approximate Computing. , 2018, , .		1
106	PUF Based Pay-Per-Device Scheme for IP Protection of CNN Model. , 2018, , .		7
107	Tetris. , 2018, , .		28
108	Leveraging DRAM Refresh to Protect the Memory Timing Channel of Cloud Chip Multi-processors. , 2018, , .		0

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109	Bias PUF based Secure Scan Chain Design. , 2018, , .		7
110	Fault tolerance on-chip: a reliable computing paradigm using self-test, self-diagnosis, and self-repair (3S) approach. Science China Information Sciences, 2018, 61, 1.	2.7	4
111	Grey Zone in Pre-Silicon Hardware Trojan Detection. , 2018, , .		4
112	RT3D: Real-Time 3-D Vehicle Detection in LiDAR Point Cloud for Autonomous Driving. IEEE Robotics and Automation Letters, 2018, 3, 3434-3440.	3.3	113
113	A retrospective evaluation of energy-efficient object detection solutions on embedded devices. , 2018, , .		9
114	Modeling attacks on strong physical unclonable functions strengthened by random number and weak PUF. , 2018, , .		18
115	SmartShuttle: Optimizing off-chip memory accesses for deep learning accelerators. , 2018, , .		66
116	STT-RAM Buffer Design for Precision-Tunable General-Purpose Neural Network Accelerator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1285-1296.	2.1	10
117	CNN-based object detection solutions for embedded heterogeneous multicore SoCs. , 2017, , .		11
118	ApproxEye: Enabling approximate computation reuse for microrobotic computer vision. , 2017, , .		3
119	ApproxPIM: Exploiting realistic 3D-stacked DRAM for energy-efficient processing in-memory. , 2017, , .		7
120	BoDNoC: Providing bandwidth-on-demand interconnection for multi-granularity memory systems. , 2017, , .		3
121	FlexFlow: A Flexible Dataflow Accelerator Architecture for Convolutional Neural Networks. , 2017, , .		217
122	Power-Utility-Driven Write Management for MLC PCM. ACM Journal on Emerging Technologies in Computing Systems, 2017, 13, 1-22.	1.8	2
123	Going Cooler With Timing-Constrained TeSHoP: A Temperature Sensing-Based Hotspot-Driven Placement Technique for FPGAs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2525-2537.	2.1	4
124	Real-Time Meets Approximate Computing. , 2017, , .		19
125	Flip-flop clustering based trace signal selection for post-silicon debug. , 2017, , .		0
126	Resilience-Aware Frequency Tuning for Neural-Network-Based Approximate Computing Chips. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2736-2748.	2.1	18

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127	Innovative practices session 10C formal verification practices in industry. , 2017, , .		0
128	Dadu. , 2017, , .		7
129	Fault diagnosis of arbiter physical unclonable function. , 2017, , .		1
130	Exploiting the Potential of Computation Reuse Through Approximate Computing. IEEE Transactions on Multi-Scale Computing Systems, 2017, 3, 152-165.	2.5	13
131	On Evaluating and Constraining Assertions Using Conflicts in Absent Scenarios. , 2017, , .		3
132	Selective off-loading to Memory. , 2017, , .		1
133	VPUF: Voter based physical unclonable function with high reliability and modeling attack resistance. , 2017, , .		17
134	Polymorphic PUF: Exploiting reconfigurability of CPU+FPGA SoC to resist modeling attack. , 2017, , .		0
135	Software-based online self-testing of network-on-chip using bounded model checking. , 2017, , .		5
136	Leveraging PVT-Margins in Design Space Exploration for FPGA-based CNN Accelerators. , 2017, , .		0
137	GeoCueDepth: Exploiting geometric structure cues to estimate depth from a single image. , 2017, , .		3
138	LAPS: Layout-Aware Path Selection for Post-Silicon Timing Characterization. IEICE Transactions on Information and Systems, 2017, E100.D, 323-331.	0.4	4
139	Polymorphic PUF: Exploiting reconfigurability of CPU+FPGA SoC to resist modeling attack. , 2017, , .		1
140	PowerTrader: Enforcing Autonomous Power Management for Future Large-Scale Many-Core Processors. IEEE Transactions on Multi-Scale Computing Systems, 2017, 3, 283-295.	2.5	1
141	Retention-Aware DRAM Assembly and Repair for Future FGR Memories. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, , 1-1.	1.9	2
142	PowerCap: Leverage Performance-Equivalent Resource Configurations for power capping. , 2016, , .		2
143	Efficient Attack on Non-linear Current Mirror PUF with Genetic Algorithm. , 2016, , .		19
144	An accurate algorithm for computing mutation coverage in model checking. , 2016, , .		3

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145	RPUF: Physical Unclonable Function with Randomized Challenge to resist modeling attack. , 2016, , .		42
146	Re-architecting the on-chip memory sub-system of machine-learning accelerator for embedded devices. , 2016, , .		16
147	ACR: Enabling computation reuse for approximate computing. , 2016, , .		9
148	Automatic Test Pattern Generation. , 2016, , 559-604.		1
149	TeSHoP: A Temperature Sensing based Hotspot-Driven Placement technique for FPGAs. , 2016, , .		1
150	DISCO. , 2016, , .		5
151	DeepBurning. , 2016, , .		158
152	Path constraint solving based test generation for observability-enhanced branch coverage. , 2016, , .		0
153	C-brain. , 2016, , .		88
154	Enhanced Wear-Rate Leveling for PRAM Lifetime Improvement Considering Process Variation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 92-102.	2.1	13
155	VANUCA: Enabling Near-Threshold Voltage Operation in Large-Capacity Cache. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 858-870.	2.1	5
156	PSI Conscious Write Scheduling: Architectural Support for Reliable Power Delivery in 3-D Die-Stacked PCM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1613-1625.	2.1	5
157	A Cost-Effective Energy Optimization Framework of Multicore SoCs Based on Dynamically Reconfigurable Voltage-Frequency Islands. ACM Transactions on Design Automation of Electronic Systems, 2016, 21, 1-14.	1.9	5
158	CoreRank: Redeeming â€œSick Siliconâ€•by Dynamically Quantifying Core-Level Healthy Condition. IEEE Transactions on Computers, 2016, 65, 716-729.	2.4	6
159	Abstraction-Guided Simulation Using Markov Analysis for Functional Verification. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 285-297.	1.9	6
160	EcoUp: Towards Economical Datacenter Upgrading. IEEE Transactions on Parallel and Distributed Systems, 2016, 27, 1968-1981.	4.0	4
161	LOFT: A low-overhead fault-tolerant routing scheme for 3D NoCs. The Integration VLSI Journal, 2016, 52, 41-50.	1.3	10
162	DTMAC: A Delay Tolerant MAC Protocol for Underwater Wireless Sensor Networks. IEEE Sensors Journal, 2016, 16, 4137-4146.	2.4	38

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163	Functional Test Generation for Hard-to-Reach States Using Path Constraint Solving. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 999-1011.	1.9	8
164	An Analytical Framework for Estimating Scale-Out and Scale-Up Power Efficiency of Heterogeneous Manycores. IEEE Transactions on Computers, 2016, 65, 367-381.	2.4	16
165	Frequency Scheduling For Resilient Chip Multi-Processors Operating at Near Threshold Voltage. , 2016, , .		0
166	DCPUF. , 2016, , .		3
167	Property Coverage Analysis Based Trustworthiness Verification for Potential Threats from EDA Tools. , 2016, , .		2
168	A Lightweight Timing Channel Protection for Shared Memory Controllers. , 2015, , .		0
169	A Similarity Based Circuit Partitioning and Trimming Method to Defend against Hardware Trojans. , 2015, , .		3
170	A signal degradation reduction method for memristor ratioed logic (MRL) gates. IEICE Electronics Express, 2015, 12, 20150062-20150062.	0.3	5
171	Temperature-Aware Software-Based Self-Testing for Delay Faults. , 2015, , .		14
172	Enhanced LCCG: A novel test clock generation scheme for faster-than-at-speed delay testing. , 2015, , .		8
173	Retraining-Based Timing Error Mitigation for Hardware Neural Networks. , 2015, , .		14
174	TWiN: A Turn-Guided Reliable Routing Scheme for Wireless 3D NoCs. , 2015, , .		1
175	OPUF: Obfuscation logic based physical unclonable function. , 2015, , .		19
176	A privacy preserving authentication scheme for roaming services in global mobility networks. Security and Communication Networks, 2015, 8, 2850-2859.	1.0	19
177	RISO: Enforce Noninterfered Performance With Relaxed Network-on-Chip Isolation in Many-Core Cloud Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 3053-3064.	2.1	2
178	An on-chip frequency programmable test clock generation and application method for small delay defect detection. The Integration VLSI Journal, 2015, 49, 87-97.	1.3	5
179	Impact assessment of net metering on smart home cyberattack detection. , 2015, , .		9
180	RADAR. , 2015, , .		9

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181	On optimizing system energy of multi-core SoCs based on dynamically reconfigurable voltage-frequency island. , 2015, , .		2
182	ShuttleNoC: Boosting on-chip communication efficiency by enabling localized power adaptation. , 2015, , .		7
183	TURO: A lightweight turn-guided routing scheme for 3D NoCs. , 2015, , .		2
184	ProPRAM. , 2015, , .		12
185	A case of precision-tunable STT-RAM memory design for approximate neural network. , 2015, , .		6
186	Data Remapping for Static NUCA in Degradable Chip Multiprocessors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 879-892.	2.1	8
187	Diagnosis and Layout Aware (DLA) Scan Chain Stitching. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 466-479.	2.1	13
188	Economizing TSV Resources in 3-D Network-on-Chip Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 493-506.	2.1	22
189	On-Chip Delay Sensor for Environments with Large Temperature Fluctuations. , 2014, , .		0
190	An On-Line Timing Error Detection Method for Silicon Debug. , 2014, , .		2
191	Short-SET: An energy-efficient write scheme for MLC PCM. , 2014, , .		4
192	SmartCap. ACM Transactions on Design Automation of Electronic Systems, 2014, 20, 1-16.	1.9	4
193	Diagnose Failures Caused by Multiple Locations at a Time. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 824-837.	2.1	12
194	HARS: A High-Performance Reliable Routing Scheme for 3D NoCs. , 2014, , .		7
195	A novel abstraction-guided simulation approach using posterior probabilities for verification. , 2014, , .		0
196	A low power DRAM refresh control scheme for 3D memory cube. , 2014, , .		3
197	Test-Quality Optimization for Variable <inline-formula> <tex-math notation="TeX">n </tex-math></inline-formula>-Detections of Transition Faults. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1738-1749.	2.1	17
198	Lifetime Enhancement Techniques for PCM-Based Image Buffer in Multimedia Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1450-1455.	2.1	12

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199	Partial-SET: Write speedup of PCM main memory. , 2014, , .		3
200	Orchestrator: Guarding Against Voltage Emergencies in Multithreaded Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2476-2487.	2.1	0
201	Data-aware DRAM refresh to squeeze the margin of retention time in hybrid memory cube. , 2014, , .		11
202	The Abacus Turn Model. , 2014, , 69-103.		1
203	Partial-SET: Write speedup of PCM main memory. , 2014, , .		1
204	Capturing Post-Silicon Variation by Layout-aware Path-delay Testing. , 2013, , .		2
205	Test Path Selection for Capturing Delay Failures Under Statistical Timing Model. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1210-1219.	2.1	14
206	Enabling Near-Threshold Voltage(NTV) operation in Multi-VDD cache for power reduction. , 2013, , .		1
207	SmartCap: User Experience-Oriented Power Adaptation for Smartphones Application Processor. , 2013, , .		8
208	RSAK: Random stream attack for phase change memory in video applications. , 2013, , .		0
209	HHC: Hierarchical hardware checkpointing to accelerate fault recovery for SRAM-based FPGAs. , 2013, , .		0
210	Path Constraint Solving Based Test Generation for Hard-to-Reach States. , 2013, , .		12
211	Orchestrator: A Low-cost Solution to Reduce Voltage Emergencies for Multi-threaded Applications. , 2013, , .		4
212	On predicting NBTI-induced circuit aging by isolating leakage change. , 2013, , .		1
213	Thermal-Constrained Task Allocation for Interconnect Energy Reduction in 3-D Homogeneous MPSoCs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 239-249.	2.1	55
214	Unified Capture Scheme for Small Delay Defect Detection and Aging Prediction. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 821-833.	2.1	17
215	Automatic Test Program Generation Using Executing-Trace-Based Constraint Extraction for Embedded Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1220-1233.	2.1	34
216	SoftPCM: Enhancing Energy Efficiency and Lifetime of Phase Change Memory in Video Applications via Approximate Write. , 2012, , .		27

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217	A clustering-based scheme for concurrent trace in debugging NoC-based multicore systems. , 2012, , .		0
218	Off-path leakage power aware routing for SRAM-based FPGAs. , 2012, , .		2
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