Xiaowei Li

List of Publications by Year in descending order

265 papers	2,724 citations	471061 17 h-index	476904 29 g-index
266 all docs	266 docs citations	266 times ranked	1819 citing authors

#	Article	IF	Citations
1	FlexFlow: A Flexible Dataflow Accelerator Architecture for Convolutional Neural Networks. , 2017, , .		217
2	DeepBurning. , 2016, , .		158
3	RT3D: Real-Time 3-D Vehicle Detection in LiDAR Point Cloud for Autonomous Driving. IEEE Robotics and Automation Letters, 2018, 3, 3434-3440.	3.3	113
4	C-brain. , 2016, , .		88
5	On Topology Reconfiguration for Defect-Tolerant NoC-Based Homogeneous Manycore Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 1173-1186.	2.1	70
6	SmartShuttle: Optimizing off-chip memory accesses for deep learning accelerators. , 2018, , .		66
7	EnGN: A High-Throughput and Energy-Efficient Accelerator for Large Graph Neural Networks. IEEE Transactions on Computers, 2021, 70, 1511-1525.	2.4	64
8	Thermal-Constrained Task Allocation for Interconnect Energy Reduction in 3-D Homogeneous MPSoCs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 239-249.	2.1	55
9	Exploring Spatial-Temporal Multi-Frequency Analysis for High-Fidelity and Temporal-Consistency Video Prediction. , 2020, , .		50
10	RPUF: Physical Unclonable Function with Randomized Challenge to resist modeling attack. , 2016, , .		42
11	AgileRegulator: A hybrid voltage regulator scheme redeeming dark silicon for power efficiency in a multicore architecture. , 2012, , .		40
12	DTMAC: A Delay Tolerant MAC Protocol for Underwater Wireless Sensor Networks. IEEE Sensors Journal, 2016, 16, 4137-4146.	2.4	38
13	Automatic Test Program Generation Using Executing-Trace-Based Constraint Extraction for Embedded Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1220-1233.	2.1	34
14	SqueezeFlow: A Sparse CNN Accelerator Exploiting Concise Convolution Rules. IEEE Transactions on Computers, 2019, 68, 1663-1677.	2.4	33
15	A High-Precision On-Chip Path Delay Measurement Architecture. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1565-1577.	2.1	30
16	Chaotic Weights: A Novel Approach to Protect Intellectual Property of Deep Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1327-1339.	1.9	29
17	Defect Tolerance in Homogeneous Manycore Processors Using Core-Level Redundancy with Unified Topology. , 2008, , .		28
18	Tetris. , 2018, , .		28

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19	SoftPCM: Enhancing Energy Efficiency and Lifetime of Phase Change Memory in Video Applications via Approximate Write. , 2012, , .		27
20	PIMSim: A Flexible and Detailed Processing-in-Memory Simulator. IEEE Computer Architecture Letters, 2019, 18, 6-9.	1.0	26
21	IVF: Characterizing the Vulnerability of Microprocessor Structures to Intermittent Faults. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 777-790.	2.1	23
22	Economizing TSV Resources in 3-D Network-on-Chip Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 493-506.	2.1	22
23	Embedded Test Decompressor to Reduce the Required Channels and Vector Memory of Tester for Complex Processor Circuit. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 531-540.	2.1	21
24	A Fault Criticality Evaluation Framework of Digital Systems for Error Tolerant Video Applications. , 2011, , .		21
25	HTDet: A clustering method using information entropy for hardware Trojan detection. Tsinghua Science and Technology, 2021, 26, 48-61.	4.1	20
26	OPUF: Obfuscation logic based physical unclonable function. , 2015, , .		19
27	A privacy preserving authentication scheme for roaming services in global mobility networks. Security and Communication Networks, 2015, 8, 2850-2859.	1.0	19
28	Efficient Attack on Non-linear Current Mirror PUF with Genetic Algorithm. , 2016, , .		19
29	Real-Time Meets Approximate Computing. , 2017, , .		19
30	Reliability Evaluation and Analysis of FPGA-Based Neural Network Acceleration System. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 472-484.	2.1	19
31	Resilience-Aware Frequency Tuning for Neural-Network-Based Approximate Computing Chips. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2736-2748.	2.1	18
32	Modeling attacks on strong physical unclonable functions strengthened by random number and weak PUF. , 2018, , .		18
33	A Low Overhead On-Chip Path Delay Measurement Circuit. , 2009, , .		17
34	Unified Capture Scheme for Small Delay Defect Detection and Aging Prediction. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 821-833.	2.1	17
35	Test-Quality Optimization for Variable <inline-formula> <tex-math notation="TeX">n </tex-math></inline-formula>-Detections of Transition Faults. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1738-1749.	2.1	17
36	VPUF: Voter based physical unclonable function with high reliability and modeling attack resistance. , 2017, , .		17

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37	Hardware Trojan in FPGA CNN Accelerator. , 2018, , .		17
38	Scan Chain Based Attacks and Countermeasures: A Survey. IEEE Access, 2019, 7, 85055-85065.	2.6	17
39	DeepBurning-GL. , 2020, , .		17
40	Statistical lifetime reliability optimization considering joint effect of process variation and aging. The Integration VLSI Journal, 2011, 44, 185-191.	1.3	16
41	Testable Path Selection and Grouping for Faster Than At-Speed Testing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 236-247.	2.1	16
42	Re-architecting the on-chip memory sub-system of machine-learning accelerator for embedded devices. , 2016, , .		16
43	An Analytical Framework for Estimating Scale-Out and Scale-Up Power Efficiency of Heterogeneous Manycores. IEEE Transactions on Computers, 2016, 65, 367-381.	2.4	16
44	Addressing the issue of processing element under-utilization in general-purpose systolic deep learning accelerators. , 2019, , .		16
45	RRAMedy: Protecting ReRAM-Based Neural Network from Permanent and Soft Faults During Its Lifetime. , 2019, , .		16
46	A Guaranteed Secure Scan Design Based on Test Data Obfuscation by Cryptographic Hash. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4524-4536.	1.9	16
47	Trajectory Tracking Based on Adaptive Sliding Mode Control for Agricultural Tractor. IEEE Access, 2020, 8, 113021-113029.	2.6	15
48	Test Path Selection for Capturing Delay Failures Under Statistical Timing Model. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1210-1219.	2.1	14
49	Temperature-Aware Software-Based Self-Testing for Delay Faults. , 2015, , .		14
50	Retraining-Based Timing Error Mitigation for Hardware Neural Networks. , 2015, , .		14
51	BZIP: A compact data memory system for UTXO-based blockchains. Journal of Systems Architecture, 2020, 109, 101809.	2.5	14
52	Happy Emotion Recognition From Unconstrained Videos Using 3D Hybrid Deep Features. IEEE Access, 2021, 9, 35524-35538.	2.6	14
53	A resilient on-chip router design through data path salvaging. , 2011, , .		13
54	Diagnosis and Layout Aware (DLA) Scan Chain Stitching. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 466-479.	2.1	13

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55	Enhanced Wear-Rate Leveling for PRAM Lifetime Improvement Considering Process Variation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 92-102.	2.1	13
56	Exploiting the Potential of Computation Reuse Through Approximate Computing. IEEE Transactions on Multi-Scale Computing Systems, 2017, 3, 152-165.	2.5	13
57	P ³ M. , 2019, , .		13
58	GramsDet: Hardware Trojan Detection Based on Recurrent Neural Network. , 2019, , .		13
59	Survey: Hardware Trojan Detection for Netlist. , 2020, , .		13
60	A Scan-Based Delay Test Method for Reduction of Overtesting. , 2008, , .		12
61	Path Constraint Solving Based Test Generation for Hard-to-Reach States. , 2013, , .		12
62	Diagnose Failures Caused by Multiple Locations at a Time. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 824-837.	2.1	12
63	Lifetime Enhancement Techniques for PCM-Based Image Buffer in Multimedia Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1450-1455.	2.1	12
64	ProPRAM. , 2015, , .		12
65	Resilient Neural Network Training for Accelerators with Computing Errors. , 2019, , .		12
66	Systolic Cube. , 2019, , .		12
67	Sequence Triggered Hardware Trojan in Neural Network Accelerator. , 2020, , .		12
68	Internet connected vehicle platoon system modeling and linear stability analysis. Computer Communications, 2021, 174, 92-100.	3.1	12
69	Test Resource Partitioning Based on Efficient Response Compaction for Test Time and Tester Channels Reduction. Journal of Computer Science and Technology, 2005, 20, 201-209.	0.9	11
70	Selection of Crosstalk-Induced Faults in Enhanced Delay Test. Journal of Electronic Testing: Theory and Applications (JETTA), 2005, 21, 181-195.	0.9	11
71	Path Delay Test Generation Toward Activation of Worst Case Coupling Effects. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1969-1982.	2.1	11
72	Data-aware DRAM refresh to squeeze the margin of retention time in hybrid memory cube. , 2014, , .		11

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73	CNN-based object detection solutions for embedded heterogeneous multicore SoCs. , 2017, , .		11
74	LMDet: A â€œNaturalnessâ€•Statistical Method for Hardware Trojan Detection. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 720-732.	2.1	11
75	InS-DLA: An In-SSD Deep Learning Accelerator for Near-Data Processing. , 2019, , .		11
76	LOFT: A low-overhead fault-tolerant routing scheme for 3D NoCs. The Integration VLSI Journal, 2016, 52, 41-50.	1.3	10
77	STT-RAM Buffer Design for Precision-Tunable General-Purpose Neural Network Accelerator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1285-1296.	2.1	10
78	A Case of On-Chip Memory Subsystem Design for Low-Power CNN Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1971-1984.	1.9	10
79	An Edge 3D CNN Accelerator for Low-Power Activity Recognition. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 918-930.	1.9	10
80	HyCA: A Hybrid Computing Architecture for Fault-Tolerant Deep Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3400-3413.	1.9	10
81	Codeword Selection for Crosstalk Avoidance and Error Correction on Interconnects. VLSI Test Symposium (VTS), Proceedings, IEEE, 2008, , .	1.0	9
82	Wrapper Chain Design for Testing TSVs Minimization in Circuit-Partitioned 3D SoC. , 2011, , .		9
83	Impact assessment of net metering on smart home cyberattack detection. , 2015, , .		9
84	RADAR. , 2015, , .		9
85	ACR: Enabling computation reuse for approximate computing. , 2016, , .		9
86	A retrospective evaluation of energy-efficient object detection solutions on embedded devices. , 2018, , .		9
87	TNPU. , 2019, , .		9
88	An Agile Precision-Tunable CNN Accelerator based on ReRAM. , 2019, , .		9
89	Software-Based Self-Testing Using Bounded Model Checking for Out-of-Order Superscalar Processors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 714-727.	1.9	9
90	SmartCap: User Experience-Oriented Power Adaptation for Smartphones Application Processor. , 2013, , .		8

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91	Enhanced LCCG: A novel test clock generation scheme for faster-than-at-speed delay testing. , 2015, , .		8
92	Data Remapping for Static NUCA in Degradable Chip Multiprocessors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 879-892.	2.1	8
93	Functional Test Generation for Hard-to-Reach States Using Path Constraint Solving. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 999-1011.	1.9	8
94	Squeezing the Last MHz for CNN Acceleration on FPGAs. , 2019, , .		8
95	Performance-asymmetry-aware topology virtualization for defect-tolerant NoC-based many-core processors. , 2010, , .		7
96	Fast path selection for testing of small delay defects considering path correlations. , 2010, , .		7
97	HARS: A High-Performance Reliable Routing Scheme for 3D NoCs. , 2014, , .		7
98	ShuttleNoC: Boosting on-chip communication efficiency by enabling localized power adaptation. , 2015, , .		7
99	ApproxPIM: Exploiting realistic 3D-stacked DRAM for energy-efficient processing in-memory. , 2017, , .		7
100	Dadu. , 2017, , .		7
101	CCR: A concise convolution rule for sparse neural network accelerators. , 2018, , .		7
102	A Low Overhead In-Network Data Compressor for the Memory Hierarchy of Chip Multiprocessors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1265-1277.	1.9	7
103	Hardware Trojan Detection Based on Signal Correlation. , 2018, , .		7
104	PUF Based Pay-Per-Device Scheme for IP Protection of CNN Model. , 2018, , .		7
105	Bias PUF based Secure Scan Chain Design. , 2018, , .		7
106	BZIP: A Compact Data Memory System for UTXO-based Blockchains. , 2019, , .		7
107	Learn-to-Scale: Parallelizing Deep Learning Inference on Chip Multiprocessor Architecture. , 2019, , .		7
108	A None-Sparse Inference Accelerator that Distills and Reuses the Computation Redundancy in CNNs. , 2019, , .		7

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109	Persistent Fault Analysis of Neural Networks on FPGA-based Acceleration System. , 2020, , .		7
110	MultiPAD: A Multivariant Partition-Based Method for Audio Adversarial Examples Detection. IEEE Access, 2020, 8, 63368-63380.	2.6	7
111	Two-Stage Safe Reinforcement Learning for High-Speed Autonomous Racing. , 2020, , .		7
112	A case of precision-tunable STT-RAM memory design for approximate neural network. , 2015, , .		6
113	CoreRank: Redeeming â€œSick Siliconâ€•by Dynamically Quantifying Core-Level Healthy Condition. IEEE Transactions on Computers, 2016, 65, 716-729.	2.4	6
114	Abstraction-Guided Simulation Using Markov Analysis for Functional Verification. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 285-297.	1.9	6
115	Accelerating DNN-based 3D point cloud processing for mobile computing. Science China Information Sciences, 2019, 62, 1.	2.7	6
116	Test Generation for Crosstalk Glitches Considering Multiple Coupling Effects. , 2007, , .		5
117	Small Delay Fault Simulation for Sequential Circuits. , 2009, , .		5
118	A signal degradation reduction method for memristor ratioed logic (MRL) gates. IEICE Electronics Express, 2015, 12, 20150062-20150062.	0.3	5
119	An on-chip frequency programmable test clock generation and application method for small delay defect detection. The Integration VLSI Journal, 2015, 49, 87-97.	1.3	5
120	DISCO. , 2016, , .		5
121	VANUCA: Enabling Near-Threshold Voltage Operation in Large-Capacity Cache. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 858-870.	2.1	5
122	PSI Conscious Write Scheduling: Architectural Support for Reliable Power Delivery in 3-D Die-Stacked PCM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1613-1625.	2.1	5
123	A Cost-Effective Energy Optimization Framework of Multicore SoCs Based on Dynamically Reconfigurable Voltage-Frequency Islands. ACM Transactions on Design Automation of Electronic Systems, 2016, 21, 1-14.	1.9	5
124	Software-based online self-testing of network-on-chip using bounded model checking. , 2017, , .		5
125	PIMCH: Cooperative memory prefetching in processing-in-memory architecture. , 2018, , .		5
126	Leveraging Memory PUFs and PIM-based encryption to secure edge deep learning systems. , 2019, , .		5

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127	SynergyFlow. ACM Transactions on Design Automation of Electronic Systems, 2019, 24, 1-27.	1.9	5
128	R2F: A Remote Retraining Framework for AIoT Processors With Computing Errors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1955-1966.	2.1	5
129	Testable Critical Path Selection Considering Process Variation. IEICE Transactions on Information and Systems, 2010, E93-D, 59-67.	0.4	5
130	KFS-LIO: Key-Feature Selection for Lightweight Lidar Inertial Odometry. , 2021, , .		5
131	INORâ€"An Intelligent noise reduction method to defend against adversarial audio examples. Neurocomputing, 2020, 401, 160-172.	3.5	5
132	A many-core accelerator design for on-chip deep reinforcement learning. , 2020, , .		5
133	Reduction of Number of Paths to be Tested in Delay Testing. Journal of Electronic Testing: Theory and Applications (JETTA), 2000, 16, 477-485.	0.9	4
134	Design-for-Testability Features and Test Implementation of a Giga Hertz General Purpose Microprocessor. Journal of Computer Science and Technology, 2008, 23, 1037-1046.	0.9	4
135	Reliable Network-on-Chip Router for Crosstalk and Soft Error Tolerance. , 2008, , .		4
136	A Scalable Scan Architecture for Godson-3 Multicore Microprocessor. , 2009, , .		4
137	Exploiting Free LUT Entries to Mitigate Soft Errors in SRAM-based FPGAs. , 2011, , .		4
138	A New Multiple-Round Dimension-Order Routing for Networks-on-Chip. IEICE Transactions on Information and Systems, 2011, E94-D, 809-821.	0.4	4
139	Flip-Flop Selection for Partial Enhanced Scan to Reduce Transition Test Data Volume. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 2157-2169.	2.1	4
140	Orchestrator: A Low-cost Solution to Reduce Voltage Emergencies for Multi-threaded Applications. , 2013, , .		4
141	Short-SET: An energy-efficient write scheme for MLC PCM. , 2014, , .		4
142	SmartCap. ACM Transactions on Design Automation of Electronic Systems, 2014, 20, 1-16.	1.9	4
143	EcoUp: Towards Economical Datacenter Upgrading. IEEE Transactions on Parallel and Distributed Systems, 2016, 27, 1968-1981.	4.0	4
144	Going Cooler With Timing-Constrained TeSHoP: A Temperature Sensing-Based Hotspot-Driven Placement Technique for FPGAs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2525-2537.	2.1	4

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146	Fault tolerance on-chip: a reliable computing paradigm using self-test, self-diagnosis, and self-repair (3S) approach. Science China Information Sciences, 2018, 61, 1.	2.7	4
147	Grey Zone in Pre-Silicon Hardware Trojan Detection. , 2018, , .		4
148	Simulate-the-hardware. , 2019, , .		4
149	PUFPass: A password management mechanism based on software/hardware codesign. The Integration VLSI Journal, 2019, 64, 173-183.	1.3	4
150	Cluster Restoration-Based Trace Signal Selection for Post-Silicon Debug. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 767-779.	1.9	4
151	TARe: Task-Adaptive in-situ ReRAM Computing for Graph Learning. , 2021, , .		4
152	Towards State-Aware Computation in ReRAM Neural Networks. , 2020, , .		4
153	A novel RTL behavioral description based ATPG method. Journal of Computer Science and Technology, 2003, 18, 308-317.	0.9	3
154	Embedded Test Resource for SoC to Reduce Required Tester Channels Based on Advanced Convolutional Codes. IEEE Transactions on Instrumentation and Measurement, 2006, 55, 389-399.	2.4	3
155	Multiple Coupling Effects Oriented Path Delay Test Generation. VLSI Test Symposium (VTS), Proceedings, IEEE, 2008, , .	1.0	3
156	T²- TAM:Reusing infrastructure resource to provide parallel testing for NoC based Chip. , 2009, , .		3
157	M-IVC: Using Multiple Input Vectors to Minimize Aging-Induced Delay. , 2009, , .		3
158	A greedy approach to tolerate defect cores for multimedia applications. , 2011, , .		3
159	A unified architecture for speed-binning and circuit failure prediction and detection. , 2012, , .		3
160	A low power DRAM refresh control scheme for 3D memory cube. , 2014, , .		3
161	Partial-SET: Write speedup of PCM main memory. , 2014, , .		3
162	A Similarity Based Circuit Partitioning and Trimming Method to Defend against Hardware Trojans. , 2015, , .		3

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163	An accurate algorithm for computing mutation coverage in model checking. , 2016, , .		3
164	ApproxEye: Enabling approximate computation reuse for microrobotic computer vision. , 2017, , .		3
165	BoDNoC: Providing bandwidth-on-demand interconnection for multi-granularity memory systems. , 2017, , .		3
166	On Evaluating and Constraining Assertions Using Conflicts in Absent Scenarios. , 2017, , .		3
167	GeoCueDepth: Exploiting geometric structure cues to estimate depth from a single image. , 2017, , .		3
168	Deterministic and Probabilistic Diagnostic Challenge Generation for Arbiter Physical Unclonable Function. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 3186-3197.	1.9	3
169	ShuttleNoC: Power-Adaptable Communication Infrastructure for Many-Core Processors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1438-1451.	1.9	3
170	ShuntFlow. , 2019, , .		3
171	Exploring emerging CNFET for efficient last level cache design. , 2019, , .		3
172	Thread: Towards fine-grained precision reconfiguration in variable-precision neural network accelerator. IEICE Electronics Express, 2019, 16, 20190145-20190145.	0.3	3
173	VNet: A Versatile Network for Efficient Real-Time Semantic Segmentation. , 2019, , .		3
174	Promoting the Harmony between Sparsity and Regularity: A Relaxed Synchronous Architecture for Convolutional Neural Networks. IEEE Transactions on Computers, 2019, 68, 867-881.	2.4	3
175	A QoS-QoR Aware CNN Accelerator Design Approach. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1995-2007.	1.9	3
176	Architecting Effectual Computation for Machine Learning Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2654-2667.	1.9	3
177	To cloud or not to cloud: an on-line scheduler for dynamic privacy-protection of deep learning workload on edge devices. CCF Transactions on High Performance Computing, 2021, 3, 85-100.	1.1	3
178	BitX: Empower Versatile Inference with Hardware Runtime Pruning. , 2021, , .		3
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182	Optimization Space Exploration of Hardware Design for CRYSTALS-KYBER. , 2020, , .		3
183	SATAM: A SAT Attack Resistant Active Metering Against IC Overbuilding. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 2025-2041.	3.2	3
184	A Voltage Template Attack on the Modular Polynomial Subtraction in Kyber. , 2022, , .		3
185	Robust test generation for power supply noise induced path delay faults. , 2008, , .		2
186	Selected Crosstalk Avoidance Code for Reliable Network-on-Chip. Journal of Computer Science and Technology, 2009, 24, 1074-1085.	0.9	2
187	Impact of Hazards on Pattern Selection for Small Delay Defects. , 2009, , .		2
188	Off-path leakage power aware routing for SRAM-based FPGAs. , 2012, , .		2
189	Capturing Post-Silicon Variation by Layout-aware Path-delay Testing. , 2013, , .		2
190	An On-Line Timing Error Detection Method for Silicon Debug. , 2014, , .		2
191	RISO: Enforce Noninterfered Performance With Relaxed Network-on-Chip Isolation in Many-Core Cloud Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 3053-3064.	2.1	2
192	On optimizing system energy of multi-core SoCs based on dynamically reconfigurable voltage-frequency island. , 2015, , .		2
193	TURO: A lightweight turn-guided routing scheme for 3D NoCs. , 2015, , .		2
194	Retention-Aware DRAM Assembly and Repair for Future FGR Memories. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, , 1-1.	1.9	2
195	PowerCap: Leverage Performance-Equivalent Resource Configurations for power capping. , 2016, , .		2
196	Power-Utility-Driven Write Management for MLC PCM. ACM Journal on Emerging Technologies in Computing Systems, 2017, 13, 1-22.	1.8	2
197	On Trace Buffer Reuse-Based Trigger Generation in Post-Silicon Debug. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2166-2179.	1.9	2
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201	GPGPU-Based ATPG System: Myth or Reality?. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 239-247.	1.9	2
202	Search-free Accelerator for Sparse Convolutional Neural Networks. , 2020, , .		2
203	CAP: Communication-aware Automated Parallelization for Deep Learning Inference on CMP Architectures. IEEE Transactions on Computers, 2021, , 1-1.	2.4	2
204	VNet: a versatile network to train real-time semantic segmentation models on a single GPU. Science China Information Sciences, 2022, 65, 1.	2.7	2
205	Property Coverage Analysis Based Trustworthiness Verification for Potential Threats from EDA Tools. , 2016, , .		2
206	Flip-Flop Selection for Transition Test Pattern Reduction Using Partial Enhanced Scan. , 2009, , .		1
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211	TeSHoP: A Temperature Sensing based Hotspot-Driven Placement technique for FPGAs. , 2016, , .		1
212	Fault diagnosis of arbiter physical unclonable function. , 2017, , .		1
213	Selective off-loading to Memory. , 2017, , .		1
214	Polymorphic PUF: Exploiting reconfigurability of CPU+FPGA SoC to resist modeling attack. , 2017, , .		1
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