## Olga Krestinskaya

## List of Publications by Year in Descending Order

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

39	412	11	19
papers	citations	h-index	g-index
53 ext. papers	603 ext. citations	<b>2.7</b> avg, IF	4.74 L-index

#	Paper	IF	Citations
39	Learning memristive spiking neurons and beyond <b>2021</b> , 517-528		
38	Analog circuit integration of backpropagation learning in memristive HTM architecture <b>2021</b> , 427-438		
37	Who is the Winner? Memristive-CMOS Hybrid Modules: CNN-LSTM Versus HTM. <i>IEEE Transactions on Biomedical Circuits and Systems</i> , <b>2020</b> , 14, 164-172	5.1	6
36	Recursive Threshold Logic-A Bioinspired Reconfigurable Dynamic Logic System With Crossbar Arrays. <i>IEEE Transactions on Biomedical Circuits and Systems</i> , <b>2020</b> , 14, 1311-1322	5.1	3
35	Automating Analogue AI Chip Design with Genetic Search. <i>Advanced Intelligent Systems</i> , <b>2020</b> , 2, 20000	76	5
34	Memristors: Properties, Models, Materials. <i>Modeling and Optimization in Science and Technologies</i> , <b>2020</b> , 13-40	0.6	4
33	HTM Theory. Modeling and Optimization in Science and Technologies, 2020, 169-180	0.6	2
32	Learning Algorithms and Implementation. <i>Modeling and Optimization in Science and Technologies</i> , <b>2020</b> , 91-102	0.6	1
31	Memristive Deep Convolutional Neural Networks. <i>Modeling and Optimization in Science and Technologies</i> , <b>2020</b> , 131-137	0.6	1
30	Memristive Hierarchical Temporal Memory. <i>Modeling and Optimization in Science and Technologies</i> , <b>2020</b> , 181-194	0.6	
29	Neuromemristive Circuits for Edge Computing: A Review. <i>IEEE Transactions on Neural Networks and Learning Systems</i> , <b>2020</b> , 31, 4-23	10.3	90
28	AMSNet: Analog Memristive System Architecture for Mean-Pooling with Dropout Convolutional Neural Network <b>2019</b> ,		1
27	Memristive Non-Idealities: Is there any Practical Implications for Designing Neural Network Chips? <b>2019</b> ,		14
26	AnalogHTM: Memristive Spatial Pooler Learning with Backpropagation 2019,		2
25	Variation-aware Binarized Memristive Networks <b>2019</b> ,		4
24	Learning in Memristive Neural Network Architectures Using Analog Backpropagation Circuits. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , <b>2019</b> , 66, 719-732	3.9	59
23	Hierarchical Temporal Memory Features with Memristor Logic Circuits for Pattern Recognition.  IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1143-1156	2.5	36

## (2017-2018)

22	Bit-Plane Extracted Moving-Object Detection Using Memristive Crossbar-CAM Arrays for Edge Computing Image Devices. <i>IEEE Access</i> , <b>2018</b> , 6, 18954-18966	3.5	17
21	A memristor-based long short term memory circuit. <i>Analog Integrated Circuits and Signal Processing</i> , <b>2018</b> , 95, 467-472	1.2	36
20	On-chip face recognition system design with memristive Hierarchical Temporal Memory. <i>Journal of Intelligent and Fuzzy Systems</i> , <b>2018</b> , 34, 1393-1402	1.6	14
19	Feature extraction without learning in an analog spatial pooler memristive-CMOS circuit design of hierarchical temporal memory. <i>Analog Integrated Circuits and Signal Processing</i> , <b>2018</b> , 95, 457-465	1.2	13
18	Image Based HTM Word Recognizer for Language Processing 2018,		1
17	Real-Time Analog Pixel-to-Pixel Dynamic Frame Differencing with Memristive Sensing Circuits 2018,		1
16	Programmable Memristive Threshold Logic Gate Array 2018,		2
15	Wafer Quality Inspection using Memristive LSTM, ANN, DNN and HTM 2018,		4
14	Notice of Retraction: Variability Analysis of Memristor-based Sigmoid Function 2018,		2
13	Notice of Retraction: Design And Analysis Of CMOS-Memristive Cascode Current Mirror 2018,		1
12	Design of CMOS-memristor Circuits for LSTM architecture 2018,		11
11	Hierarchical Temporal Memory Using Memristor Networks: A Survey. <i>IEEE Transactions on Emerging Topics in Computational Intelligence</i> , <b>2018</b> , 2, 380-395	4.1	22
10	Notice of Retraction: Perceptron Linear Activation Function Design with CMOS-Memristive Circuits <b>2018</b> ,		1
9	Notice of Retraction: Analysis of Multilayer Perceptron with Rectifier Linear Unit Activation Function <b>2018</b> ,		2
8	Introduction to Memristive HTM Circuits 2018,		9
7	Analog Backpropagation Learning Circuits for Memristive Crossbar Neural Networks 2018,		25
6	Design and implication of a rule based weight sparsity module in HTM spatial pooler 2017,		3
5	Neuromorphic Adaptive Edge-Preserving Denoising Filter <b>2017</b> ,		3

4	Unified Model for Contrast Enhancement and Denoising <b>2017</b> ,	3
3	Facial emotion recognition using min-max similarity classifier 2017,	9
2	Bioinspired memory model for HTM face recognition <b>2016</b> ,	2
1	Memristor load current mirror circuit <b>2015</b> ,	2