Abdel-Hameed A Badawy

List of Publications by Year
in descending order

43 papers	279 citations	1307594 7 h-index	1281871 11 g-index
43 all docs	43 docs citations	43 times ranked	200 citing authors

#	Article	IF	Citations
1	A Divide-and-Conquer Approach to Dicke State Preparation. IEEE Transactions on Quantum Engineering, 2022, 3, 1-16.	4.9	12
2	Hardware Trojan Insertion Using Reinforcement Learning. , 2022, , .		5
3	A Survey on the Security of Wired, Wireless, and 3D Network-on-Chips. IEEE Access, 2021, 9, 107625-107656.	4.2	16
4	Joint security and performance improvement in multilevel shared caches. IET Information Security, 2021, 15, 297-308.	1.7	0
5	Load-Aware Dynamic Time Synchronization in Parallel Discrete Event Simulation. , 2021, , .		3
6	Securing network-on-chips via novel anonymous routing. , 2021, , .		8
7	Hybrid, scalable, trace-driven performance modeling of GPGPUs. , 2021, , .		7
8	NVIDIA GPGPUs Instructions Energy Consumption. , 2020, , .		0
9	FQ-AGO: Fuzzy Logic Q-Learning Based Asymmetric Link Aware and Geographic Opportunistic Routing Scheme for MANETs. Electronics (Switzerland), 2020, 9, 576.	3.1	11
10	Energy-Efficient Ternary Multipliers Using CNT Transistors. Electronics (Switzerland), 2020, 9, 643.	3.1	15
11	Verified instruction-level energy consumption measurement for NVIDIA GPUs. , 2020, , .		13
12	Fast, accurate, and scalable memory modeling of GPGPUs using reuse profiles. , 2020, , .		11
13	PPT-SASMM: Scalable Analytical Shared Memory Model. , 2020, , .		2
14	High performance, variation-tolerant CNFET ternary full adder a process, voltage, and temperature variation-resilient design. Computers and Electrical Engineering, 2019, 77, 205-216.	4.8	20
15	PPT-GPU: Scalable GPU Performance Modeling. IEEE Computer Architecture Letters, 2019, 18, 55-58.	1.5	22
16	FPGA-Accelerated Decision Tree Classifier for Real-Time Supervision of Bluetooth SoC. , 2019, , .		3
17	GPUs Cache Performance Estimation using Reuse Distance Analysis. , 2019, , .		5
18	Machine Learning Bluetooth Profile Operation Verification via Monitoring the Transmission Pattern. , 2019, , .		0

#	Article	IF	Citations
19	Low Overhead Instruction Latency Characterization for NVIDIA GPGPUs. , 2019, , .		9
20	POSTER: GPUs Pipeline Latency Analysis. , 2019, , .		0
21	A performance study of the time-varying cache behavior: a study on APEX, Mantevo, NAS, and PARSEC. Journal of Supercomputing, 2018, 74, 665-695.	3.6	1
22	A Scalable Analytical Memory Model for CPU Performance Prediction. Lecture Notes in Computer Science, 2018, , 114-135.	1.3	6
23	Fault Tolerance Performance Evaluation of Large-Scale Distributed Storage Systems HDFS and Ceph Case Study. , 2018, , .		3
24	StAdHyTM: A Statically Adaptive Hybrid Transactional Memory: A scalability study on large parallel graphs. , 2017, , .		2
25	Optimizing thin client caches for mobile cloud computing:. Concurrency Computation Practice and Experience, 2017, 29, e4048.	2.2	6
26	Design of adiabatic MTJ-CMOS hybrid circuits. , 2017, , .		3
27	Optical computing. Nanophotonics, 2017, 6, 503-505.	6.0	42
28	A brief history of HPC simulation and future challenges. , 2017, , .		3
29	A Probabilistic Monte Carlo Framework for Branch Prediction. , 2017, , .		7
30	Enabling energy-efficient ternary logic gates using CNFETs. , 2017, , .		16
31	Analyzing Hybrid Transactional Memory Performance Using Intel SDE. , 2017, , .		0
32	Optimizing locality in graph computations using reuse distance profiles. , 2017, , .		3
33	Probabilistic Monte Carlo simulations for static branch prediction. , 2017, , .		1
34	Local memory store (LMStr): A hardware controlled shared scratchpad for multicores. , 2017, , .		2
35	DAdHTM: Low overhead dynamically adaptive hardware transactional memory for large graphs a scalability study. , 2017, , .		2
36	Guiding Locality Optimizations for Graph Computations via Reuse Distance Analysis. IEEE Computer Architecture Letters, 2017, 16, 119-122.	1.5	4

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37	Spare block cache (SprBlk): Fault resilience and reliability at low voltages. , 2017, , .		1
38	LMStr. , 2017, , .		1
39	The time-varying nature of cache utilization: A case study on the Mantevo and Apex benchmarks. , 2017, , .		1
40	LMStr: Local memory store the case for hardware controlled scratchpad memory for general purpose processors. , 2016, , .		6
41	Cache Utilization as a Locality Metric - A Case Study on the Mantevo Suite. , 2016, , .		5
42	Let There Be Hope: Assessing the Implications of Exam Re-Taking on Student Learning Outcomes and Grades of Engineering Students Grounded on Metacognition Awareness Framework. , 2016, , .		0
43	PPT-Multicore: performance prediction of OpenMP applications using reuse profiles and analytical modeling. Journal of Supercomputing, 0, , 1.	3.6	2