Hironori Kasahara

List of Publications by Year
in descending order

85	734	759190 12	642715 23
papers	citations	h-index	g-index

92	92	92	478
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A standard task graph set for fair evaluation of multiprocessor scheduling algorithms. Journal of Scheduling, 2002, 5, 379-394.	1.9	143
2	Humanoid Robots in Waseda Universityâ€"Hadaly-2 and WABIAN. Autonomous Robots, 2002, 12, 25-38.	4.8	75
3	Stem Cell-derived Neural Stem/Progenitor Cell Supporting Factor Is an Autocrine/Paracrine Survival Factor for Adult Neural Stem/Progenitor Cells. Journal of Biological Chemistry, 2003, 278, 35491-35500.	3.4	47
4	An 8640 MIPS SoC with Independent Power-Off Control of 8 CPUs and 8 RAMs by An Automatic Parallelizing Compiler. , 2008, , .		36
5	A 45nm 37.3GOPS/W heterogeneous multi-core SoC. , 2010, , .		27
6	Automatic Coarse Grain Task Parallel Processing on SMP Using OpenMP. Lecture Notes in Computer Science, 2001, , 189-207.	1.3	26
7	A 4320MIPS Four-Processor Core SMP/AMP with Individually Managed Clock Frequency for Low Power Consumption. Digest of Technical Papers - IEEE International Solid-State Circuits Conference, 2007, , .	0.0	25
8	Hierarchical Parallelism Control for Multigrain Parallel Processing. Lecture Notes in Computer Science, 2005, , 31-44.	1.3	23
9	Job scheduling scheme for pure space sharing among rigid jobs. Lecture Notes in Computer Science, 1998, , 98-121.	1.3	22
10	OSCAR API for Real-Time Low-Power Multicores and Its Performance on Multicores and SMP Servers. Lecture Notes in Computer Science, 2010, , 188-202.	1.3	20
11	What Will 2022 Look Like? The IEEE CS 2022 Report. Computer, 2015, 48, 68-76.	1.1	19
12	Heterogeneous Multi-Core Architecture That Enables 54x AAC-LC Stereo Encoding. IEEE Journal of Solid-State Circuits, 2008, 43, 902-910.	5.4	17
13	Coarse grain parallelism detection scheme of a fortran program. Systems and Computers in Japan, 1991, 22, 24-36.	0.2	16
14	Compiler Control Power Saving Scheme for Multi Core Processors. Lecture Notes in Computer Science, 2006, , 362-376.	1.3	16
15	Computer Education in the Age of COVID-19. Computer, 2020, 53, 114-118.	1.1	15
16	Coarse Grain Task Parallel Processing with Cache Optimization on Shared Memory Multiprocessor. Lecture Notes in Computer Science, 2003, , 352-365.	1.3	13
17	Performance of OSCAR Multigrain Parallelizing Compiler on SMP Servers. Lecture Notes in Computer Science, 2005, , 319-331.	1.3	12
18	Data-localization for Fortran macro-dataflow computation using partial static task assignment. , 1996, , .		11

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19	A data-localization compilation scheme using partial-static task assignment for Fortran coarse-grain parallel processing. Parallel Computing, 1998, 24, 579-596.	2.1	10
20	Cache Optimization for Coarse Grain Task Parallel Processing Using Inter-Array Padding. Lecture Notes in Computer Science, 2004, , 64-76.	1.3	9
21	Language Extensions in Support of Compiler Parallelization. Lecture Notes in Computer Science, 2007, , 78-94.	1.3	9
22	A parallel optimization algorithm for minimum executionâ€time multiprocessor scheduling problem. Systems and Computers in Japan, 1992, 23, 54-65.	0.2	8
23	Multigrain Parallelization for Model-Based Design Applications Using the OSCAR Compiler. Lecture Notes in Computer Science, 2016, , 125-139.	1.3	8
24	Practical multiprocessor scheduling algorithms for efficient parallel processing. Systems and Computers in Japan, 1985, 16, 11-19.	0.2	7
25	Heterogeneous Multiprocessor on a Chip Which Enables 54x AAC-LC Stereo Encoding. , 2007, , .		7
26	Parallelization with Automatic Parallelizing Compiler Generating Consumer Electronics Multicore API. , 2008, , .		7
27	Multicore Cache Coherence Control by a Parallelizing Compiler. , 2017, , .		7
28	Coarse-grain Task Parallel Processing Using the OpenMP Backend of the OSCAR Multigrain Parallelizing Compiler. Lecture Notes in Computer Science, 2000, , 457-470.	1.3	7
29	Parallel processing scheme for robot control computation using multi-processor scheduling algorithm.. Journal of the Robotics Society of Japan, 1984, 2, 387-401.	0.1	7
30	Parallel processing of robot arm dynamic control computation on multimicroprocessors. Microprocessors and Microsystems, 1990, 14, 3-9.	2.8	5
31	Parallelization of automotive engine control software on embedded multi-core processor using OSCAR compiler. , 2013, , .		5
32	Data localization using loop aligned decomposition for macro-dataflow processing. Lecture Notes in Computer Science, 1997, , 56-74.	1.3	5
33	Engineering Education in the Age of Autonomous Machines. Computer, 2021, 54, 66-69.	1.1	4
34	A Parallelizing Compiler Cooperative Heterogeneous Multicore Processor Architecture. Lecture Notes in Computer Science, 2011, , 215-233.	1.3	4
35	Static Coarse Grain Task Scheduling with Cache Optimization Using OpenMP. International Journal of Parallel Programming, 2003, 31, 211-223.	1.5	3
36	Reconciling application power control and operating systems for optimal power and performance. , 2013, , .		3

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37	Accelerating Multicore Architecture Simulation Using Application Profile. , 2016, , .		3
38	Parallel processing scheme of a basic block in a fortran program on oscar. Systems and Computers in Japan, 1991, 22, 1-13.	0.2	2
39	Evaluation of Power Consumption at Execution of Multiple Automatically Parallelized and Power Controlled Media Applications on the RP2 Low-Power Multicore. Lecture Notes in Computer Science, 2013, , 31-45.	1.3	2
40	Reducing parallelizing compilation time by removing redundant analysis. , 2016, , .		2
41	Cascaded DMA Controller for Speedup of Indirect Memory Access in Irregular Applications. , 2019, , .		2
42	Parallel Processing of Hybrid Finite Element and Boundary Element Method for Electro-magnetic Field Analysis. IEEJ Transactions on Fundamentals and Materials, 1998, 118, 373-379.	0.2	2
43	PARALLEL PROCESSING OF ROBOT CONTROL AND SIMULATION. World Scientific Series in Robotics and Intelligent Systems, 1992, , 77-93.	0.1	2
44	Automatic Local Memory Management for Multicores Having Global Address Space. Lecture Notes in Computer Science, 2017, , 282-296.	1.3	2
45	Performance Evaluation of Compiler Controlled Power Saving Scheme. , 2005, , 480-493.		2
46	Application of df/ihs to minimum total weighted flow time multiprocessor scheduling problems. Systems and Computers in Japan, 1988, 19, 25-34.	0.2	1
47	Application of parallel processing to PWR plant predictive simulator.. Nippon Genshiryoku Gakkaishi/Journal of the Atomic Energy Society of Japan, 1990, 32, 1009-1022.	0.0	1
48	Power-Aware Compiler Controllable Chip Multiprocessor. Parallel Architecture and Compilation Techniques (PACT), Proceedings of the International Conference on, 2007, , .	0.0	1
49	Software-cooperative power-efficient heterogeneous multi-core for media processing. , 2008, , .		1
50	Multiple-Paths Search with Concurrent Thread Scheduling for Fast AND/OR Tree Search. , 2009, , .		1
51	Green Multicore-SoC Software-Execution Framework with Timely-Power-Gating Scheme. , 2009, , .		1
52	Automatic parallelization, performance predictability and power control for mobile-applications. , 2013, , .		1
53	Parallelization of tree-to-TLV serialization. , 2014, , .		1
54	Annotatable systrace: an extended Linux ftrace for tracing a parallelized program. , 2015, , .		1

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55	Architecture Design for the Environmental Monitoring System over the Winter Season. , 2016, , .		1
56	Guest Editorial: Special Issue on Network and Parallel Computing for Emerging Architectures and Applications. International Journal of Parallel Programming, 2019, 47, 343-344.	1.5	1
57	Collaboration for the Future. Computer, 2019, 52, 72-76.	1.1	1
58	Compiler Software Coherent Control for Embedded High Performance Multicore. IEICE Transactions on Electronics, 2020, E103.C, 85-97.	0.6	1
59	OSCAR Parallelizing and Power Reducing Compiler and API for Heterogeneous Multicores : (Invited) Tj ETQq1 1 0.784314 rgBT /Overlo		1
60	Task scheduling algorithms for multiprocessor realâ€time control systems. Electrical Engineering in Japan (English Translation of Denki Gakkai Ronbunshi), 1987, 107, 120-130.	0.4	0
61	Parallel Processing of Robot Dynamics Simulation Using Optimal Multiprocessor Scheduling Algorithms. Systems and Computers in Japan, 1988, 19, 45-54.	0.2	0
62	Power reduction controll for multicores in OSCAR multigrain parallelizing compiler. , 2008, , .		0
63	A 45-nm 37.3 GOPS/W Heterogeneous Multi-Core SOC with 16/32 Bit Instruction-Set General-Purpose Core. IEICE Transactions on Electronics, 2011, E94-C, 663-669.	0.6	0
64	Enhancing the performance of a multiplayer game by using a parallelizing compiler. , 2012, , .		0
65	Processor Cores. , 2012, , 19-122.		0
66	Dynamic Profiling and Feedback Framework for Reduce-Side Join. , 2013, , .		0
67	Android Video Processing System Combined with Automatically Parallelized and Power Optimized Code by OSCAR Compiler. Journal of Information Processing, 2016, 24, 504-511.	0.4	0
68	Message from the CAP 2017 Organizing Committee. , 2017, , .		0
69	Satisfaction and Sustainability. Computer, 2018, 51, 4-6.	1.1	0
70	Fast and Highly Optimizing Separate Compilation for Automatic Parallelization. , 2019, , .		0
71	Multicore Processors for Consumer Electronics. Journal of the Institute of Electrical Engineers of Japan, 2008, 128, 172-175.	0.0	0
72	Application Programs and Systems. , 2012, , 179-218.		0

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73	Parallel Processing of MENDEL Using Multiprocessor Scheduling Algorithms. IEEJ Transactions on Electronics, Information and Systems, 1987, 107, 149-156.	0.2	0
74	Research Prospect of Multiprocessor Systems. IEEJ Transactions on Electronics, Information and Systems, 1988, 108, 96-103.	0.2	0
75	Perspective on advanced parallel processing system for robotics.. Journal of the Robotics Society of Japan, 1988, 6, 318-325.	0.1	0
76	Preface to the Special Issue on Parallel Processing Technology. IEEJ Transactions on Electronics, Information and Systems, 1993, 113, 905-905.	0.2	0
77	Parallel Processing of Continuous/Discrete-Time Control Systems Simulation. IEEJ Transactions on Electronics, Information and Systems, 1993, 113, 939-946.	0.2	0
78	Parallel Processing of Non-Linear Equations Solution on Multiprocessor Systems. IEEJ Transactions on Electronics, Information and Systems, 1993, 113, 947-954.	0.2	0
79	III. Software for Parallel Processing. IEEJ Transactions on Electronics, Information and Systems, 1993, 113, 919-927.	0.2	0
80	Near Fine Grain Parallel Processing of Circuit Simulation Using Direct Method. IEEJ Transactions on Electronics, Information and Systems, 1994, 114, 579-587.	0.2	0
81	Application of Parallel Processing to Power System Analysis. IEEJ Transactions on Power and Energy, 1997, 117, 621-624.	0.2	0
82	Coarse Grain Task Parallelization of Earthquake Simulator GMS Using OSCAR Compiler on Various Cc-NUMA Servers. Lecture Notes in Computer Science, 2016, , 238-253.	1.3	0
83	Software Cache Coherent Control byÂParallelizing Compiler. Lecture Notes in Computer Science, 2019, , 17-25.	1.3	0
84	Local Memory Mapping of Multicore Processors on an Automatic Parallelizing Compiler. IEICE Transactions on Electronics, 2020, E103.C, 98-109.	0.6	0
85	Performance Evaluation of OSCAR Multi-target Automatic Parallelizing Compiler on Intel, AMD, Arm and RISC-V Multicores. Lecture Notes in Computer Science, 2022, , 50-64.	1.3	0