

Denis Flandre

List of Publications by Year in descending order

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664
papers

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57719

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times ranked

5257
citing authors

#	ARTICLE	IF	CITATIONS
1	Analysis and Design of RF Energy-Harvesting Systems With Impedance-Aware Rectifier Sizing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2023, 70, 361-365.	2.2	4
2	Characterization of thin Al ₂ O ₃ /SiO ₂ dielectric stack for CMOS transistors. Microelectronic Engineering, 2022, 254, 111708.	1.1	10
3	An Ultra-Thin Ultraviolet Enhanced Backside-Illuminated Single-Photon Avalanche Diode With 650 nm-Thin Silicon Body Based on SOI Technology. IEEE Journal of Selected Topics in Quantum Electronics, 2022, 28, 1-10.	1.9	2
4	Comprehensive Analytical Comparison of Ring Oscillators in FDSOI Technology: Current Starving Versus Back-Bias Control. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 1883-1895.	3.5	6
5	An Ultra-Low-Power Read-Out Circuit for Interfacing Novel Gas Sensors Matrices. IEEE Sensors Journal, 2022, 22, 9521-9533.	2.4	7
6	Accurate and Insightful Closed-Form Prediction of Subthreshold SRAM Hold Failure Rate. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 2767-2780.	3.5	1
7	Design-Window Methodology for Inductorless Noise-Cancelling CMOS LNAs. IEEE Access, 2022, 10, 29482-29492.	2.6	3
8	Spike-Based Sensing and Communication for Highly Energy-Efficient Sensor Edge Nodes. , 2022, , .		4
9	High-performance dual-mode ultra-thin broadband CdS/CIGS heterojunction photodetector on steel. Optics Express, 2022, 30, 13875.	1.7	11
10	Characteristics of noise degradation and recovery in gamma-irradiated SOI nMOSFET with in-situ thermal annealing. Solid-State Electronics, 2022, , 108300.	0.8	0
11	Low-power silicon strain sensor based on CMOS current reference topology. Sensors and Actuators A: Physical, 2022, 339, 113491.	2.0	0
12	SiO _x Patterned Based Substrates Implemented in Cu(In,Ga)Se ₂ Ultrathin Solar Cells: Optimum Thickness. IEEE Journal of Photovoltaics, 2022, 12, 954-961.	1.5	4
13	Investigation and optimization of traps properties in Al ₂ O ₃ /SiO ₂ dielectric stacks using conductance method. Solid-State Electronics, 2022, 194, 108347.	0.8	2
14	Experimental study of thermal coupling effects in FD-SOI MOSFET. Solid-State Electronics, 2022, 194, 108362.	0.8	1
15	Correlation and optimization of the optoelectrical properties of DC magnetron-sputtered Cu ₂ ZnSnS ₄ absorber layer as a function of the material composition. Materials Science in Semiconductor Processing, 2021, 121, 105367.	1.9	4
16	Extensive Electrical Characterization Methodology of Advanced MOSFETs Towards Analog and RF Applications. IEEE Journal of the Electron Devices Society, 2021, 9, 500-510.	1.2	9
17	A Physical Model of Contact Resistance in Ti-Contacted Graphene-Based Field Effect Transistors. IEEE Transactions on Electron Devices, 2021, 68, 892-898.	1.6	4
18	15.3: Defect Engineering in In ₂ O ₃ Type Oxide Semiconductor TFTs. Digest of Technical Papers SID International Symposium, 2021, 52, 101-101.	0.1	0

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19	A Wearable Low-Power Sensing Platform for Environmental and Health Monitoring: The Convergence Project. <i>Sensors</i> , 2021, 21, 1802.	2.1	12
20	Determination of Carrier Lifetime in Silicon Using an Ultra-thin Al ₂ O ₃ /SiO ₂ Dielectric Stack. , 2021, , .		1
21	Depletion effects in moderately doped TiO ₂ layers from C-V characteristics of MIS structures on Si. <i>Applied Physics Express</i> , 2021, 14, 051008.	1.1	1
22	Improved Split CV Mobility Extraction in 28 nm Fully Depleted Silicon on Insulator Transistors. <i>IEEE Electron Device Letters</i> , 2021, 42, 661-664.	2.2	2
23	High-responsivity broadband photodetection of an ultra-thin In ₂ S ₃ /CIGS heterojunction on steel. <i>Optics Letters</i> , 2021, 46, 2288.	1.7	7
24	Comparative Study of Al ₂ O ₃ and HfO ₂ for Surface Passivation of Cu(In,Ga)Se ₂ Thin Films: An Innovative Al ₂ O ₃ /HfO ₂ Multistack Design. <i>Physica Status Solidi (A) Applications and Materials Science</i> , 2021, 218, 2100073.	0.8	5
25	The shift of breakdown voltage for silicon membrane strip detectors resulting from surface avalanche. <i>Journal of Applied Physics</i> , 2021, 129, 214501.	1.1	0
26	A Self-Gating RF Energy Harvester for Wireless Power Transfer With High-PAPR Incident Waveform. <i>IEEE Journal of Solid-State Circuits</i> , 2021, 56, 1816-1826.	3.5	11
27	SleepRunner: A 28-nm FDSOI ULP Cortex-M0 MCU With ULL SRAM and UFBR PVT Compensation for 2.6-3.6-µW/DMIPS 40-80-MHz Active Mode and 131-nW/kB Fully Retentive Deep-Sleep Mode. <i>IEEE Journal of Solid-State Circuits</i> , 2021, 56, 2256-2269.	3.5	18
28	Trap Recovery by in-Situ Annealing in Fully-Depleted MOSFET With Active Silicide Resistor. <i>IEEE Electron Device Letters</i> , 2021, 42, 1085-1088.	2.2	6
29	Origin of low-temperature negative transconductance in multilayer MoS ₂ transistors. <i>Applied Physics Letters</i> , 2021, 119, .	1.5	1
30	Indirect light absorption model for highly strained silicon infrared sensors. <i>Journal of Applied Physics</i> , 2021, 130, .	1.1	6
31	29.3: Invited Paper: Defect Engineering in n-Type Oxide Semiconductor TFTs. <i>Digest of Technical Papers SID International Symposium</i> , 2021, 52, 400-400.	0.1	0
32	Perovskite Metal-Oxide Semiconductor Structures for Interface Characterization. <i>Advanced Materials Interfaces</i> , 2021, 8, 2101004.	1.9	1
33	Temperature-dependent performance of Schottky-Barrier FET ultra-low-power diode. <i>Solid-State Electronics</i> , 2021, 184, 108124.	0.8	0
34	High-Performance and Industrially Viable Nanostructured SiO _x Layers for Interface Passivation in Thin Film Solar Cells. <i>Solar Rrl</i> , 2021, 5, 2000534.	3.1	15
35	The Impact of LCE and PAMDLE Regarding Different CMOS ICs Nodes and High Temperatures. <i>IEEE Journal of the Electron Devices Society</i> , 2021, 9, 415-423.	1.2	5
36	Non-Linear Output-Conductance Function for Robust Analysis of Two-Dimensional Transistors. <i>IEEE Electron Device Letters</i> , 2021, 42, 94-97.	2.2	2

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37	Bottom-Up Life-Cycle Assessment of MEMS Piezoresistive Pressure Sensors. , 2021, , .		0
38	In-situ recovery of on-membrane PD-SOI MOSFET from TID defects after gamma irradiation. , 2021, , .		0
39	Perovskite Metalâ€“Oxideâ€“Semiconductor Structures for Interface Characterization (Adv. Mater.) Tj ETQq1 1 0.784314 rgBT /Overl	1.9	1
40	Ultra-Thinned Individual SOI Die ACF FC Bonded on Rigid and Flex PCB. , 2021, , .		0
41	Improving MOSFET Piezoresistive Strain Gauges Limit of Detection Using Lock-In Principle. , 2021, , .		0
42	Learning with Physical Noise or Errors. IEEE Transactions on Dependable and Secure Computing, 2020, 17, 957-971.	3.7	3
43	Ultralow Power Ionizing Dose Sensor Based on Complementary Fully Depleted MOS Transistors for Radiotherapy Application. IEEE Transactions on Nuclear Science, 2020, 67, 2217-2223.	1.2	2
44	Impact of hydrogen dopant incorporation on InGaZnO, ZnO and In₂O₃ thin film transistors. Physical Chemistry Chemical Physics, 2020, 22, 1591-1597.	1.3	16
45	Electrodes-oxide-semiconductor device for biosensing: Renewed conformal analysis and multilayer algorithm. Journal of Electroanalytical Chemistry, 2020, 856, 113651.	1.9	3
46	A method for threshold voltage extraction in junctionless MOSFETs using the derivative of transconductance-to-current ratio. Solid-State Electronics, 2020, 168, 107723.	0.8	6
47	A 2.5-GHz Clock Recovery Circuit Based on a Back-Bias-Controlled Oscillator in 28-nm FDSOI. IEEE Solid-State Circuits Letters, 2020, 3, 478-481.	1.3	1
48	Low-Frequency Noise Analysis Of On-Membrane Mosfet And In-Situ Thermal Annealing. , 2020, , .		3
49	New Universal Figure of Merit for Embedded Si Piezoresistive Pressure Sensors. IEEE Sensors Journal, 2020, , 1-1.	2.4	5
50	Optimization of Back Contact Grid Size in Al₂O₃-Rear-Passivated Ultrathin CIGS PV Cells by 2-D Simulations. IEEE Journal of Photovoltaics, 2020, 10, 1908-1917.	1.5	24
51	Enhanced Ultraviolet Avalanche Photodiode With 640-nm-Thin Silicon Body Based on SOI Technology. IEEE Transactions on Electron Devices, 2020, 67, 4641-4644.	1.6	10
52	Black phosphorus field effect transistors stable in harsh conditions via surface engineering. Applied Physics Letters, 2020, 117, .	1.5	7
53	Design Considerations of Ultra-Low-Power Polymer Gas Microsensors Based on Noise Analysis. Proceedings (mdpi), 2020, 56, .	0.2	2
54	Experimental results on diodes and BIMOS ESD devices in 28Ånm FD-SOI under TLP & TID radiation. Microelectronics Reliability, 2020, 114, 113938.	0.9	0

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55	High Voltage Gain WSe_2 Complementary Compact Inverter With Buried Gate for Local Doping. IEEE Electron Device Letters, 2020, 41, 944-947.	2.2	14
56	28-nm FD-SOI CMOS RF Figures of Merit Down to 4.2 K. IEEE Journal of the Electron Devices Society, 2020, 8, 646-654.	1.2	27
57	Self-Heating in FDSOI UTBB MOSFETs at Cryogenic Temperatures and its Effect on Analog Figures of Merit. IEEE Journal of the Electron Devices Society, 2020, 8, 789-796.	1.2	11
58	Structural and Opto-electronic characterization of CuO thin films prepared by DC reactive magnetron sputtering. Journal of Materials Science: Materials in Electronics, 2020, 31, 4563-4573.	1.1	8
59	Performances Evaluation of On-Chip Large-Size-Tapped Transformer for MEMS Applications. IEEE Transactions on Instrumentation and Measurement, 2020, 69, 7051-7060.	2.4	5
60	Electrical characterization of advanced MOSFETs towards analog and RF applications. , 2020, , .		1
61	Schottky-Barrier FET Ultra-Low-Power Diode. , 2020, , .		0
62	Micrometer-thin SOI Sensors for E-Skin Applications. , 2020, , .		1
63	Anisotropic conductive film & flip-chip bonding for low-cost sensor prototyping on rigid & flex PCB. , 2020, , .		1
64	Methodology for Performance Optimization in Noise- and Distortion-Canceling LNA. , 2019, , .		4
65	Low-Power, High-Sensitivity Temperature Sensor Based on Ultrathin SOI Lateral p-i-n Gated Diode. IEEE Transactions on Electron Devices, 2019, 66, 4001-4007.	1.6	3
66	Analysis, Modeling, and Design of a 2.45-GHz RF Energy Harvester for SWIPT IoT Smart Sensors. IEEE Journal of Solid-State Circuits, 2019, 54, 2717-2729.	3.5	41
67	Detection mechanism in highly sensitive ZnO nanowires network gas sensors. Sensors and Actuators B: Chemical, 2019, 297, 126602.	4.0	28
68	A security oriented transient-noise simulation methodology: Evaluation of intrinsic physical noise of cryptographic designs. The Integration VLSI Journal, 2019, 68, 71-79.	1.3	3
69	Light management design in ultra-thin chalcopyrite photovoltaic devices by employing optical modelling. Solar Energy Materials and Solar Cells, 2019, 200, 109933.	3.0	21
70	Defect Self-Compensation for High-Mobility Bilayer InGaZnO/In ₂ O ₃ Thin-Film Transistor. Advanced Electronic Materials, 2019, 5, 1900125.	2.6	43
71	Exploring and suppressing the kink effect of black phosphorus field-effect transistors operating in the saturation regime. Nanoscale, 2019, 11, 10420-10428.	2.8	8
72	28-nm FDSOI nMOSFET RF Figures of Merits and Parasitic Elements Extraction at Cryogenic Temperature Down to 77 K. IEEE Journal of the Electron Devices Society, 2019, 7, 810-816.	1.2	12

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73	28-nm FDSOI analog and RF Figures of Merit at N2 cryogenic temperatures. Solid-State Electronics, 2019, 159, 77-82.	0.8	21
74	Enhanced ultraviolet photoresponse in a graphene-gated ultra-thin Si-based photodiode. Journal Physics D: Applied Physics, 2019, 52, 245101.	1.3	10
75	Ultra Low-Loss Si Substrate for On-Chip UWB GHz Antennas. IEEE Journal of the Electron Devices Society, 2019, 7, 393-397.	1.2	7
76	A battery-less BLE smart sensor for room occupancy tracking supplied by 2.45-GHz wireless power transfer. The Integration VLSI Journal, 2019, 67, 8-18.	1.3	17
77	Back-gate bias Effect on the MOSFET-C CMOS UTBB Performance by Circuit Simulations. , 2019, , .		3
78	gm/ID-derivative Method for Threshold Voltage Extraction in Junctionless MOSFETs. , 2019, , .		0
79	Robust Methodology for Low-Frequency Noise Power Analyses in Advanced MOS Transistors. , 2019, , .		4
80	Self-Heating in 28 FDSOI UTBB MOSFETs at Cryogenic Temperatures. , 2019, , .		4
81	Harmonic Distortion in Symmetric and Asymmetric Self-Cascodes of UTBB FD SOI Planar MOSFETs. , 2019, , .		0
82	Subthreshold Operation of Self-Cascade Structure Using UTBB FD SOI Planar MOSFETs. , 2019, , .		1
83	Low-Frequency Noise Transistor Performance for UTBB FDSOI MOSFET-C Filters. , 2019, , .		2
84	Live Demonstration: A Highly Selective Temperature and Humidity Compensated MOX Based Multi-Gas Sensor Module with Bluetooth 5.0 Connectivity. , 2019, , .		0
85	28 FDSOI RF Figures of Merit down to 4.2 K. , 2019, , .		5
86	Surface Passivation of CIGS Solar Cells Using Gallium Oxide. Physica Status Solidi (A) Applications and Materials Science, 2018, 215, 1700826.	0.8	36
87	Analysis and Specification of an IR-UWB Transceiver for High-Speed Chip-to-Chip Communication in a Server Chassis. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 2015-2023.	3.5	11
88	Multilevel Half-Rate Phase Detector for Clock and Data Recovery Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1807-1811.	2.1	5
89	A Low-Power and In Situ Annealing Technique for the Recovery of Active Devices After Proton Irradiation. EPJ Web of Conferences, 2018, 170, 01006.	0.1	3
90	A Robust 10-Gb/s Duobinary Transceiver in 0.13-µm SOI CMOS for Short-Haul Optical Networks. IEEE Transactions on Industrial Electronics, 2018, 65, 1518-1525.	5.2	2

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91	Development, characterisation and simulation of wafer bonded Si-on-SiC substrates. Materials Science in Semiconductor Processing, 2018, 78, 69-74.	1.9	12
92	Intrinsic rectification in common-gated graphene field-effect transistors. Nano Energy, 2018, 43, 37-46.	8.2	10
93	28 FDSOI RF Figures of Merits and Parasitic Elements at Cryogenic Temperature. , 2018, , .		0
94	8-T ULV SRAM macro in 28nm FDSOI with 7.4 pW/bit retention power and back-biased-scalable speed/energy trade-off. , 2018, , .		5
95	Design of a 2.45-GHz RF Energy Harvester for SWIPT IoT smart sensors. , 2018, , .		4
96	A Transient Noise Analysis of Secured Dual-Rail Based Logic Style. , 2018, , .		0
97	Using Statistical Student's t-Test to Qualify the Electrical Performance of the Diamond MOSFETs. , 2018, , .		1
98	Asymmetric Self-Cascode Current-Voltage Constructing Algorithm for Analog Figures-of-Merit Extraction. , 2018, , .		0
99	Numerical Simulation and Analysis of Transistor Channel Length and Doping Mismatching in GC SOI nMOSFETs Analog Figures of Merit. , 2018, , .		0
100	Linearity Enhancement in Asymmetric Self-Cascode Composed by FD SOI nMOSFETs. , 2018, , .		0
101	A Battery-Less BLE IoT Motion Detector Supplied by 2.45-GHz Wireless Power Transfer. , 2018, , .		9
102	Fully-Depleted SOI MOSFET Sensors in Accumulation Mode for Total Dose Measurement. , 2018, , .		2
103	28 FDSOI analog and RF Figures of Merit at cryogenic temperatures. , 2018, , .		7
104	Low-power half-rate dual-loop clock-recovery system in 28-nm FDSOI. , 2018, , .		3
105	Understanding hydrogen and nitrogen doping on active defects in amorphous In-Ga-Zn-O thin film transistors. Applied Physics Letters, 2018, 112, .	1.5	28
106	Wafer-Scale Nanoimprint Lithography Process Towards Complementary Silicon Nanowire Field-Effect Transistors for Biosensor Applications. Physica Status Solidi (A) Applications and Materials Science, 2018, 215, 1800234.	0.8	10
107	Gradient importance sampling: An efficient statistical extraction methodology of high-sigma SRAM dynamic characteristics. , 2018, , .		16
108	Design benefits of self-cascode configuration for analog applications in 28 FDSOI. , 2018, , .		1

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109	Quantum Efficiency Improvement of SOI p-i-n Lateral Diodes Operating as UV Detectors at High Temperatures. IEEE Sensors Journal, 2017, 17, 1641-1648.	2.4	5
110	Boosting the SOI MOSFET Electrical Performance by Using the Octagonal Layout Style in High Temperature Environment. IEEE Transactions on Device and Materials Reliability, 2017, 17, 221-228.	1.5	6
111	Multiple-Wavelength Detection in SOI Lateral PIN Diodes With Backside Reflectors. IEEE Transactions on Industrial Electronics, 2017, 64, 7368-7376.	5.2	6
112	A Quasi-Static Model of Silicon Substrate Effects in Graphene Field Effect Transistors. IEEE Electron Device Letters, 2017, 38, 987-990.	2.2	5
113	<i>In-situ</i> thermal annealing of on-membrane silicon-on-insulator semiconductor-based devices after high gamma dose irradiation. Nanotechnology, 2017, 28, 184001.	1.3	9
114	Optimisation of rear reflectance in ultra-thin CIGS solar cells towards >20% efficiency. Solar Energy, 2017, 146, 443-452.	2.9	38
115	Reliable characteristics and stabilization of on-membrane SOI MOSFET-based components heated up to 335 Å°C. Semiconductor Science and Technology, 2017, 32, 014001.	1.0	9
116	Leakage Current and Low-Frequency Noise Analysis and Reduction in a Suspended SOI Lateral p-i-n Diode. IEEE Transactions on Electron Devices, 2017, 64, 4252-4259.	1.6	8
117	Design and Fabrication of Silicon-on-Silicon-Carbide Substrates and Power Devices for Space Applications. E3S Web of Conferences, 2017, 16, 12003.	0.2	1
118	Addressing the impact of rear surface passivation mechanisms on ultra-thin Cu(In,Ga)Se ₂ solar cell performances using SCAPS 1-D model. Solar Energy, 2017, 157, 603-613.	2.9	45
119	Scaling Trends for Dual-Rail Logic Styles Against Side-Channel Attacks: A Case-Study. Lecture Notes in Computer Science, 2017, , 19-33.	1.0	8
120	Comparative study of non-linearities in 28 nm node FDSOI and Bulk MOSFETs. , 2017, , .		9
121	Back-gate bias effect on FDSOI MOSFET RF Figures of Merits and parasitic elements. , 2017, , .		9
122	Automated layout-integrated sizing of a 2.45 GHz differential-drive rectifier in 28 nm FDSOI CMOS. , 2017, , .		0
123	RF SOI CMOS technology on 1st and 2nd generation trap-rich high resistivity SOI wafers. Solid-State Electronics, 2017, 128, 121-128.	0.8	13
124	An in-depth analysis of temperature effect on DIBL in UTBB FD SOI MOSFETs based on experimental data, numerical simulations and analytical models. Solid-State Electronics, 2017, 128, 67-71.	0.8	2
125	An 80-MHz 0.4V ULV SRAM macro in 28nm FDSOI achieving 28-fJ/bit access energy with a ULP bitcell and on-chip adaptive back bias generation. , 2017, , .		9
126	High-efficiency wireless power transfer for mm-size biomedical implants. , 2017, , .		5

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127	Improving noise and linearity of CMOS wideband inductorless balun LNAs for 10-GHz software-defined radios in 28nm FDSOI. , 2017, , .		2
128	Back-gate bias effect on UTBB-FDSOI non-linearity performance. , 2017, , .		5
129	Single event effects and total ionising dose in 600V Si-on-SiC LDMOS transistors for rad-hard space applications. , 2017, , .		5
130	Channel width influence on the analog performance of the asymmetric self-cascode FD SOI nMOSFETs. , 2017, , .		1
131	Experimental evaluation of mismatching on the analog characteristics of GC SOI MOSFETs. , 2017, , .		1
132	Comparative experimental study of the improved MOSFETs matching by using the hexagonal layout style. , 2017, , .		1
133	Effect of the back bias on the analog performance of standard FD and UTBB transistors-based self-cascode structures. Semiconductor Science and Technology, 2017, 32, 095005.	1.0	2
134	Artificial Microsystems for Sensing Airflow, Temperature, and Humidity by Combining MEMS and CMOS Technologies. , 2017, , 243-256.		0
135	Origin of the Low-Frequency Noise in the Asymmetric Self-Cascode Structure Composed by Fully Depleted SOI nMOSFETs. Journal of Integrated Circuits and Systems, 2017, 12, 62-70.	0.3	1
136	Experimental and simulation analysis of electrical characteristics of commonâ€source current mirrors implemented with asymmetric selfâ€cascode siliconâ€onâ€insulator nâ€channel metalâ€oxideâ€semiconductor 0.9 fieldâ€effect transistors. IET Circuits, Devices and Systems, 2016, 10, 349-355.		2
137	Boosting the MOSFETs matching by using diamond layout style. , 2016, , .		4
138	Efficient passive energy harvesters at 950 MHz and 2.45 GHz for 100 Î¼W applications in 65 nm CMOS. , 2016, , .		1
139	Low power highly linear temperature sensor based on SOI lateral PIN diodes. , 2016, , .		4
140	Use of back gate bias to improve the performance of n- and p-type UTBB transistors-based self-cascode structures applied to current mirrors. , 2016, , .		3
141	Operation of suspended lateral SOI PIN photodiode with aluminum back gate. , 2016, , .		5
142	Analysis and modelling of temperature effect on DIBL in UTBB FD SOI MOSFETs. , 2016, , .		3
143	Automated Design of a 13.56 MHz 19 Î¼W Passive Rectifier With 72% Efficiency Under 10 Î¼A load. IEEE Journal of Solid-State Circuits, 2016, 51, 1290-1301.	3.5	22
144	Electronic properties of negatively charged SiOx films deposited by Atmospheric Pressure Plasma Liquid Deposition for surface passivation of p-type c-Si solar cells. Thin Solid Films, 2016, 611, 74-77.	0.8	1

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145	CAMEL , 2016, , .		0
146	Role of Ionic Strength in Staphylococcal Cell Aggregation. Langmuir, 2016, 32, 7277-7283.	1.6	11
147	Low-frequency noise in asymmetric self-cascode FD SOI nMOSFETs. , 2016, , .		0
148	Improved operation of graded-channel SOI nMOSFETs down to liquid helium temperature. Semiconductor Science and Technology, 2016, 31, 114005.	1.0	4
149	Junctionless nanowire transistors operation at temperatures down to 4.2 K. Semiconductor Science and Technology, 2016, 31, 114001.	1.0	17
150	Automated design of a 13.56 MHz corner-robust efficient differential drive rectifier for 10 \hat{I} /4A load. , 2016, , .		3
151	A hybrid graphene-metal oxide sensor for formaldehyde detection at room temperature. , 2016, , .		0
152	Low-frequency noise of submicron graded-channel SOI nMOSFETs at high temperature. , 2016, , .		0
153	Assessment of 28 nm UTBB FD-SOI technology platform for RF applications: Figures of merit and effect of parasitic elements. Solid-State Electronics, 2016, 117, 130-137.	0.8	45
154	On the improvement of DC analog characteristics of FD SOI transistors by using asymmetric self-cascode configuration. Solid-State Electronics, 2016, 117, 152-160.	0.8	18
155	RF SOI CMOS technology on 1st and 2nd generation trap-rich high resistivity SOI wafers. , 2016, , .		1
156	A review of special gate coupling effects in long-channel SOI MOSFETs with lightly doped ultra-thin bodies and their compact analytical modeling. Solid-State Electronics, 2016, 117, 66-76.	0.8	14
157	Silicon-on-Insulator Photodiode on Micro-Hotplate Platform With Improved Responsivity and High-Temperature Application. IEEE Sensors Journal, 2016, 16, 3017-3024.	2.4	13
158	Quantitative characterization of biofunctionalization layers by robust image analysis for biosensor applications. Sensors and Actuators B: Chemical, 2016, 222, 980-986.	4.0	4
159	Capacitive Biosensing of Bacterial Cells: Sensitivity Optimization. IEEE Sensors Journal, 2016, 16, 586-595.	2.4	10
160	Comparison of self-heating and its effect on analogue performance in 28 nm bulk and FDSOI. Solid-State Electronics, 2016, 115, 219-224.	0.8	21
161	A 16 x 16 CMOS Capacitive Biosensor Array Towards Detection of Single Bacterial Cell. IEEE Transactions on Biomedical Circuits and Systems, 2016, 10, 364-374.	2.7	61
162	Towards Securing Low-Power Digital Circuits with Ultra-Low-Voltage Vdd Randomizers. Lecture Notes in Computer Science, 2016, , 233-248.	1.0	4

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163	Investigating the electronic properties of Al ₂ O ₃ /Cu(In,Ga)Se ₂ interface. AIP Advances, 2015, 5, .	0.6	69
164	A low-power and in situ annealing mitigation technique for fast neutrons irradiation of integrated temperature sensing diodes. , 2015, , .		3
165	Highly reflective rear surface passivation design for ultra-thin Cu(In,Ga)Se ₂ solar cells. Thin Solid Films, 2015, 582, 300-303.	0.8	51
166	Study of Total Quantum Efficiency of Lateral SOI PIN Photodiodes with Back-Gate Bias, Intrinsic Length and Temperature Variation. ECS Transactions, 2015, 66, 101-107.	0.3	2
167	Resonant dielectrophoresis and electrohydrodynamics for high-sensitivity impedance detection of whole-cell bacteria. Lab on A Chip, 2015, 15, 3183-3191.	3.1	17
168	Trigate nanowire MOSFETs analog figures of merit. Solid-State Electronics, 2015, 112, 78-84.	0.8	15
169	Analog performance improvement of self-cascode structures composed by UTBB transistors using back gate bias. , 2015, , .		6
170	Advantages of subthreshold operation of asymmetric self-cascode SOI transistors aiming at analog circuit applications. , 2015, , .		2
171	Boosting the total ionizing dose tolerance of digital switches by using OCTO SOI MOSFET. Semiconductor Science and Technology, 2015, 30, 105024.	1.0	11
172	A 0.48mm ² 5μW-10mW indoor/outdoor PV energy-harvesting management unit in a 65nm SoC based on a single bidirectional multi-gain/multi-mode switched-cap converter with supercap storage. , 2015, , .		6
173	Comparative study of parasitic elements on RF FoM in 28 nm FD SOI and bulk technologies. , 2015, , .		8
174	Can we connect trillions of IoT sensors in a sustainable way? A technology/circuit perspective (Invited). , 2015, , .		30
175	Use of back gate bias to enhance the analog performance of planar FD and UTBB SOI transistors-based self-cascode structures. , 2015, , .		3
176	Wide band study of silicon-on-insulator photodiodes on suspended micro-hotplates platforms. , 2015, , .		5
177	Towards ultra-low-voltage wideband noise-cancelling LNAs in 28nm FDSOI. , 2015, , .		6
178	A Capacitance-to-Frequency Converter With On-Chip Passivated Microelectrodes for Bacteria Detection in Saline Buffers Up to 575 MHz. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 159-163.	2.2	32
179	Capacitive biosensing of bacterial cells: Analytical model and numerical simulations. Sensors and Actuators B: Chemical, 2015, 211, 428-438.	4.0	32
180	Influence of Ga/(Ga + In) grading on deepμdefect states of Cu(In,Ga)Se ₂ solar cells. Physica Status Solidi - Rapid Research Letters, 2015, 9, 157-160.	1.2	14

#	ARTICLE	IF	CITATIONS
181	Wide frequency band assessment of 28nm FDSOI technology platform for analogue and RF applications. Solid-State Electronics, 2015, 108, 47-52.	0.8	29
182	Diamond layout style impact on SOI MOSFET in high temperature environment. Microelectronics Reliability, 2015, 55, 783-788.	0.9	21
183	An analytical 3D model for short-channel effects in undoped FinFETs. Journal of Computational Electronics, 2015, 14, 500-505.	1.3	5
184	Asymmetric Self-Cascode versus Graded-Channel SOI nMOSFETs for analog applications. , 2015, , .		1
185	Effect of channel doping concentration on the harmonic distortion of asymmetric n- and p-type self-cascode MOSFETs. , 2015, , .		0
186	Analysis and optimization for dynamic read stability in 28nm SRAM bitcells. , 2015, , .		0
187	Self-heating in 28 nm bulk and FDSOI. , 2015, , .		3
188	Impact of Using the Octagonal Layout for SOI MOSFETs in a High-Temperature Environment. IEEE Transactions on Device and Materials Reliability, 2015, 15, 626-628.	1.5	9
189	A 65 nm 0.5 V DPS CMOS Image Sensor With 17 pJ/Frame.Pixel and 42 dB Dynamic Range for Ultra-Low-Power SoCs. IEEE Journal of Solid-State Circuits, 2015, 50, 2419-2430.	3.5	27
190	Lytic enzymes as selectivity means for label-free, microfluidic and impedimetric detection of whole-cell bacteria using ALD-Al ₂ O ₃ passivated microelectrodes. Biosensors and Bioelectronics, 2015, 67, 154-161.	5.3	30
191	Filamentous Phages Displaying Multivalent Peptide Motives With Specific Affinity To Anodic Alumina Surfaces. Journal of Biosensors & Bioelectronics, 2015, 06, .	0.4	0
192	A 65 nm CMOS Ultra-Low-Power Impulse Radio-Ultra-Wideband Emitter for Short-Range Indoor Localization. Journal of Low Power Electronics, 2015, 11, 349-358.	0.6	3
193	The Influence of Back Gate Bias on the OCTO SOI MOSFET™s Response to X-ray Radiation. Journal of Integrated Circuits and Systems, 2015, 10, 43-48.	0.3	4
194	A Self-Oscillating System to Measure the Conductivity and the Permittivity of Liquids within a Single Triangular Signal. Journal of Sensors, 2014, 2014, 1-11.	0.6	4
195	Assessment of Global Variability in UTBB MOSFETs in Subthreshold Regime. Journal of Low Power Electronics and Applications, 2014, 4, 201-213.	1.3	8
196	Analysis of harmonic distortion of asymmetric self-cascode association of SOI nMOSFETs operating in saturation. , 2014, , .		3
197	Compact diamond MOSFET model accounting for PAMDLE applicable down 150Ånm node. Electronics Letters, 2014, 50, 1618-1620.	0.5	23
198	Using diamond layout style to boost MOSFET frequency response of analogue IC. Electronics Letters, 2014, 50, 398-400.	0.5	20

#	ARTICLE	IF	CITATIONS
199	Compensation of total ionizing dose effects in ULV SoCs through adaptive voltage scaling. , 2014, , .		1
200	Dependence of the optimum length of light doped region of GC SOI nMOSFET with front gate bias. , 2014, , .		0
201	Boosting the radiation hardness and higher reestablishing pre-rad conditions by using OCTO layout style for MOSFETs. , 2014, , .		0
202	Effect of high temperature on analog parameters of Asymmetric Self-Cascode SOI nMOSFETs. , 2014, , .		0
203	Temperature and back-gate bias influence on the operation of lateral SOI PIN photodiodes. , 2014, , .		0
204	The effects of gamma irradiation on micro-hotplates with integrated temperature sensing diodes. Proceedings of SPIE, 2014, , .	0.8	1
205	28 nm FD SOI Technology Platform RF FoM. , 2014, , .		5
206	Deposition of a SiO _x Film Showing Enhanced Surface Passivation. Energy Procedia, 2014, 55, 769-776.	1.8	3
207	Variability of UTBB MOSFET analog figures of merit in wide frequency range. , 2014, , .		3
208	Gate leakage currents model for FinFETs implemented in Verilog- π for electronic circuits design. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2014, 27, 846-862.	1.2	2
209	Analog operation of Junctionless Nanowire Transistors down to liquid helium temperature. , 2014, , .		0
210	Illuminated to dark ratio improvement in lateral SOI PIN photodiodes at high temperatures. Semiconductor Science and Technology, 2014, 29, 075008.	1.0	18
211	Effect of the temperature on on Junctionless Nanowire Transistors electrical parameters down to 4K. , 2014, , .		6
212	Efficient ultra low power rectification at 13.56 MHz for a 10 μ A load current. , 2014, , .		2
213	Asymmetric self-cascode FD SOI nMOSFETS harmonic distortion at cryogenic temperatures. , 2014, , .		1
214	On the gm/ID-based approaches for threshold voltage extraction in advanced MOSFETs and their application to ultra-thin body SOI MOSFETs. Solid-State Electronics, 2014, 97, 52-58.	0.8	17
215	A modified gm/ID design methodology for deeply scaled CMOS technologies. Analog Integrated Circuits and Signal Processing, 2014, 78, 771-784.	0.9	17
216	Out-of-plane MEMS-based mechanical airflow sensor co-integrated in SOI CMOS technology. Sensors and Actuators A: Physical, 2014, 206, 67-74.	2.0	21

#	ARTICLE	IF	CITATIONS
217	Wide frequency band assessment of 28 nm FDSOI technology platform for analogue and RF applications. , 2014, , .		16
218	A 65nm 1V to 0.5V linear regulator with ultra low quiescent current for mixed-signal ULV SoCs. , 2014, , .		3
219	Employing Si solar cell technology to increase efficiency of ultra-thin Cu(In,Ga)Se ₂ solar cells. Progress in Photovoltaics: Research and Applications, 2014, 22, 1023-1029.	4.4	136
220	A Sizing Methodology for On-Chip Switched-Capacitor DC/DC Converters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 1597-1606.	3.5	26
221	Switched-capacitor DC/DC converters for empowering Internet-of-Things SoCs. , 2014, , .		6
222	Understanding the limitations and improving the relevance of SPICE simulations in side-channel security evaluations. Journal of Cryptographic Engineering, 2014, 4, 187-195.	1.5	9
223	Assessment of different functionalization methods for grafting a protein to an alumina-covered biosensor. Biofabrication, 2014, 6, 035007.	3.7	6
224	Effect of parasitic elements on UTBB FD SOI MOSFETs RF figures of merit. Solid-State Electronics, 2014, 97, 38-44.	0.8	36
225	Tuning the surface conditioning of trapezoidally shaped silicon nanowires by (3-aminopropyl)triethoxysilane. Applied Physics Letters, 2014, 104, 023502.	1.5	6
226	Technological parameters scaling influence on the analog performance of Graded-Channel SOI nMOSFET transistors. , 2014, , .		3
227	Characterization of high-efficiency multi-crystalline silicon in industrial production. Solar Energy Materials and Solar Cells, 2013, 117, 225-230.	3.0	26
228	Asymmetric channel doping profile and temperature reduction influence on the performance of current mirrors implemented with FD SOI nMOSFETs. Microelectronics Reliability, 2013, 53, 848-855.	0.9	5
229	An ultra-low-power UWB IR pulse receiver using 65nm CMOS technology. , 2013, , .		3
230	Detector of abrupt current variations on power lines. Electronics Letters, 2013, 49, 901-903.	0.5	1
231	Low frequency noise in submicron Graded-Channel SOI MOSFETs. , 2013, , .		3
232	Characterization of ultra-thin silicon strip detectors for hadrontherapy beam monitoring. , 2013, , .		1
233	Threshold voltage extraction techniques and temperature effect in context of global variability in UTBB mosfets. , 2013, , .		3
234	Technology development on P-type silicon strip detectors for proton beam dosimetry. , 2013, , .		1

#	ARTICLE	IF	CITATIONS
235	Green SoCs for a sustainable Internet-of-Things. , 2013, , .		37
236	UTBB SOI MOSFETs analog figures of merit: Effects of ground plane and asymmetric double-gate regime. Solid-State Electronics, 2013, 90, 56-64.	0.8	44
237	Charge collection mapping of a novel ultra-thin silicon strip detector for hadrontherapy beam monitoring. Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2013, 732, 556-559.	0.7	2
238	Signal-to-noise ratio optimization for detecting bacteria with interdigitated microelectrodes. Sensors and Actuators B: Chemical, 2013, 189, 43-51.	4.0	38
239	SleepWalker: A 25-MHz 0.4-V Sub- μm^2 7- $\mu\text{W}/\text{MHz}$ Microcontroller in 65-nm LP/GP CMOS for Low-Carbon Wireless Sensor Nodes. IEEE Journal of Solid-State Circuits, 2013, 48, 20-32.	3.5	112
240	Quasi-double gate regime to boost UTBB SOI MOSFET performance in analog and sleep transistor applications. Solid-State Electronics, 2013, 84, 28-37.	0.8	10
241	Experimental comparative study between the diamond MOSFET and its conventional counterpart in high temperatures environment. , 2013, , .		9
242	Global variability of UTBB MOSFET in subthreshold. , 2013, , .		0
243	High temperature and radiation hard CMOS SOI sub-threshold voltage reference. , 2013, , .		8
244	Improved modeling of gate leakage currents for fin-shaped field-effect transistors. Journal of Applied Physics, 2013, 113, .	1.1	5
245	Ultra-Low Power High Temperature and Radiation Hard Complementary Metal-Oxide-Semiconductor (CMOS) Silicon-on-Insulator (SOI) Voltage Reference. Sensors, 2013, 13, 17265-17280.	2.1	9
246	Operation of Lateral SOI PIN Photodiodes with Back-Gate Bias and Intrinsic Length Variation. ECS Transactions, 2013, 53, 121-126.	0.3	6
247	VALIDATION OF A NOVEL ULTRA-THIN SILICON STRIP DETECTOR FOR HADRON THERAPY BEAM MONITORING. Journal of Circuits, Systems and Computers, 2013, 22, 1340018.	1.0	3
248	Analog Behavior of Submicron Graded-Channel SOI MOSFETs Varying Channel Length, Doping Concentration and Temperature. ECS Transactions, 2013, 53, 149-154.	0.3	1
249	Passivation effects of atomic-layer-deposited aluminum oxide. EPJ Photovoltaics, 2013, 4, 45107.	0.8	54
250	Total ionizing dose effects on the digital performance of irradiated OCTO and conventional fully depleted SOI MOSFET. , 2013, , .		6
251	Improving the X-ray radiation tolerance of the analog ICs by using OCTO layout style. , 2013, , .		6
252	Channel length influence on the analog characteristics of asymmetric self-cascode association of SOI transistors. , 2013, , .		10

#	ARTICLE	IF	CITATIONS
253	Impact of radiations on the electromechanical properties of materials and on the piezoresistive and capacitive transduction mechanisms used in microsystems. Proceedings of SPIE, 2013, , .	0.8	0
254	Operation of Lateral SOI PIN Photodiodes with Back-Gate Bias and Intrinsic Length Variation. ECS Meeting Abstracts, 2013, , .	0.0	0
255	Review on double-gate MOSFETs and FinFETs modeling. Facta Universitatis - Series Electronics and Energetics, 2013, 26, 197-213.	0.6	5
256	Design and characterisation of ultra-low-power SOI-CMOS IC temperature level detector. Electronics Letters, 2012, 48, 842.	0.5	3
257	Liquid Helium Temperature Operation of Graded-Channel SOI nMOSFETs. ECS Transactions, 2012, 49, 135-144.	0.3	0
258	Analytic modeling of gate tunneling currents for nano-scale double-gate MOSFETs. , 2012, , .		2
259	Room temperature atomic layer deposition of Al ₂ O ₃ and replication of butterfly wings for photovoltaic application. Journal of Vacuum Science and Technology A: Vacuum, Surfaces and Films, 2012, 30, .	0.9	15
260	Ultra-thin silicon strip detectors for hadrontherapy beam monitoring. , 2012, , .		0
261	RF behavior of undoped channel ultra-thin body with ultra-thin BOX MOSFETs. , 2012, , .		4
262	Analog performance of asymmetric self-cascode p-channel fully depleted SOI transistors. , 2012, , .		6
263	Experimental Validation of the Drain Current Analytical Model of the Fully Depleted Diamond SOI nMOSFETs by Using Paired T-test Statistical Evaluation. ECS Transactions, 2012, 49, 169-176.	0.3	0
264	Experimental Study of the OCTO SOI nMOSFET and Its Application in Analog Integrated Circuits. ECS Transactions, 2012, 49, 527-534.	0.3	6
265	On the UTBB SOI MOSFET performance improvement in quasi-double-gate regime. , 2012, , .		11
266	Compact small-signal model for RF FinFETs. , 2012, , .		5
267	Analog performance of submicron GC SOI MOSFETs. , 2012, , .		3
268	Bacteria Detection with Interdigitated Microelectrodes: Noise Consideration and Design Optimization. Procedia Engineering, 2012, 47, 188-191.	1.2	3
269	On extraction of self-heating features in UTBB SOI MOSFETs. , 2012, , .		15
270	A Compact Model for Single Event Effects in PD SOI Sub-Micron MOSFETs. IEEE Transactions on Nuclear Science, 2012, 59, 943-949.	1.2	11

#	ARTICLE	IF	CITATIONS
271	Quasi-double gate mode for sleep transistors in UTBB FD SOI low-power high-speed applications. , 2012, , .		4
272	Improvement of high-frequency FinFET performance by fin width engineering. , 2012, , .		8
273	Ultra-low-power analog and digital circuits and microsystems using disruptive ultra-low-leakage design techniques. , 2012, , .		1
274	Discrete Random Dopant Fluctuation Impact on Nanoscale Dopant-Segregated Schottky-Barrier Nanowires. IEEE Electron Device Letters, 2012, 33, 1228-1230.	2.2	11
275	Dew-Based Wireless Mini Module for Respiratory Rate Monitoring. IEEE Sensors Journal, 2012, 12, 699-706.	2.4	7
276	Liquid helium temperature analog operation of asymmetric self-cascode FD SOI MOSFETs. , 2012, , .		4
277	A dual-mode DC/DC converter for ultra-low-voltage microcontrollers. , 2012, , .		4
278	Low temperature assembly method of microfluidic bio-molecules detection device. , 2012, , .		2
279	Analysis of Dynamic Differential Swing Limited Logic for Low-Power Secure Applications. Journal of Low Power Electronics and Applications, 2012, 2, 98-126.	1.3	4
280	A 25MHz 7μW/MHz ultra-low-voltage microcontroller SoC in 65nm LP/GP CMOS for low-carbon wireless sensor nodes. , 2012, , .		21
281	High-energy neutrons effect on strained and non-strained SOI MuGFETs and planar MOSFETs. Microelectronics Reliability, 2012, 52, 118-123.	0.9	2
282	Scaling laws and performance improvements of integrated biosensor microarrays with multi-pixel per spot. Sensors and Actuators B: Chemical, 2012, 166-167, 184-192.	4.0	6
283	Impact of self-heating and substrate effects on small-signal output conductance in UTBB SOI MOSFETs. Solid-State Electronics, 2012, 71, 93-100.	0.8	46
284	Ultra-thin body and thin-BOX SOI CMOS technology analog figures of merit. Solid-State Electronics, 2012, 70, 50-58.	0.8	50
285	Extended MASTAR Modeling of DIBL in UTB and UTBB SOI MOSFETs. IEEE Transactions on Electron Devices, 2012, 59, 247-251.	1.6	36
286	Pushing Adaptive Voltage Scaling Fully on Chip. Journal of Low Power Electronics, 2012, 8, 95-112.	0.6	6
287	SOME MITIGATIONS FOR UNEQUAL DATA VARIANCE IN LINEAR REGRESSION. Series on Advances in Mathematics for Applied Sciences, 2012, , 118-125.	0.0	0
288	Design of an Ultra-Low-Power Multi-Stage AC/DC Voltage Rectifier and Multiplier Using a Fully-Automated and Portable Design Methodology. Journal of Low Power Electronics, 2012, 8, 197-206.	0.6	4

#	ARTICLE	IF	CITATIONS
289	Modeling of Thin-Film Lateral SOI PIN Diodes with an Alternative Multi-Branch Explicit Current Model. Journal of Integrated Circuits and Systems, 2012, 7, 92-99.	0.3	1
290	Characterization of Thin-Film SOI PIN Diodes from Cryogenic to Above Room Temperatures Using an Explicit I-V Multi-Branch Model. ECS Transactions, 2011, 39, 171-178.	0.3	2
291	A SOI CMOS smart strain sensor. , 2011, , .		2
292	Comparison of small-signal output conductance frequency dependence in UTBB SOI MOSFETs with and without ground plane. , 2011, , .		9
293	Ultra-high-efficiency co-integrated photovoltaic energy scavenger. , 2011, , .		2
294	Asymmetric self-cascode configuration to improve the analog performance of SOI nMOS transistors. , 2011, , .		21
295	Charge sensitive amplifier study in 2um FD SOI CMOS. , 2011, , .		3
296	Energy-Band Engineering for Improved Charge Retention in Fully Self-Aligned Double Floating-Gate Single-Electron Memories. Nano Letters, 2011, 11, 4520-4526.	4.5	22
297	A Novel Approach for Active Pressure Sensors in Thin Film SOI Technology. Procedia Engineering, 2011, 25, 43-46.	1.2	3
298	Neutron and Gamma Radiation Effects on MEMS Structures. Procedia Engineering, 2011, 25, 172-175.	1.2	2
299	A Self-Tuning Inductive Powering System for Biomedical Implants. Procedia Engineering, 2011, 25, 1585-1588.	1.2	18
300	Influence of drain voltage on MOSFET threshold voltage determination by transconductance change and g_m methods. , 2011, , .		1
301	Pre-silicon 22/20 nm compact MOSFET models for bulk vs. FD SOI low-power circuit benchmarks. , 2011, , .		3
302	Method for fabricating third generation photovoltaic cells based on Si quantum dots using ion implantation into SiO ₂ . Journal of Applied Physics, 2011, 109, .	1.1	16
303	A compact model for Single Event Effects in PD SOI sub-micron MOSFETs. , 2011, , .		0
304	Fully-Automated and Portable Design Methodology for Optimal Sizing of Energy-Efficient CMOS Voltage Rectifiers. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2011, 1, 141-149.	2.7	18
305	Design of Thin-Film Lateral SOI PIN Photodiodes with up to Tens of GHz Bandwidth. , 2011, , .		4
306	Computational study of dopant segregated nanoscale Schottky barrier MOSFETs for steep slope, low SD-resistance and high on-current gate-modulated resonant tunneling FETs. Solid-State Electronics, 2011, 65-66, 123-129.	0.8	14

#	ARTICLE	IF	CITATIONS
307	Characterization and modelling of single event transients in LDMOS-SOI FETs. Microelectronics Reliability, 2011, 51, 2004-2009.	0.9	4
308	On the MOSFET Threshold Voltage Extraction by Transconductance and Transconductance-to-Current Ratio Change Methods: Part I – Effect of Gate-Voltage-Dependent Mobility. IEEE Transactions on Electron Devices, 2011, 58, 4172-4179.	1.6	48
309	On the MOSFET Threshold Voltage Extraction by Transconductance and Transconductance-to-Current Ratio Change Methods: Part II – Effect of Drain Voltage. IEEE Transactions on Electron Devices, 2011, 58, 4180-4188.	1.6	49
310	Harvesting the potential of nano-CMOS for lightweight cryptography: an ultra-low-voltage 65Ånm AES coprocessor for passive RFID tags. Journal of Cryptographic Engineering, 2011, 1, 79-86.	1.5	29
311	3D simulation of triple-gate MOSFETs with different mobility regions. Microelectronic Engineering, 2011, 88, 1633-1636.	1.1	8
312	TRAPPISTe pixel sensor with 21¼m SOI technology. Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2011, 633, S19-S21.	0.7	5
313	Impact of neutron irradiation on the RF properties of oxidized high-resistivity silicon substrates with and without a trap-rich passivation layer. Microelectronics Reliability, 2011, 51, 326-331.	0.9	3
314	A new interdigitated array microelectrode-oxide-silicon sensor with label-free, high sensitivity and specificity for fast bacteria detection. Sensors and Actuators B: Chemical, 2011, 156, 578-587.	4.0	40
315	Gate-edge charges related effects and performance degradation in advanced multiple-gate MOSFETs. Solid-State Electronics, 2011, 59, 18-24.	0.8	11
316	Physics of Gate Modulated Resonant Tunneling (RT)-FETs: Multi-barrier MOSFET for steep slope and high on-current. Solid-State Electronics, 2011, 59, 50-61.	0.8	23
317	Self-heating and substrate effects in ultra-thin body ultra-thin BOX devices. , 2011, , .		11
318	Innovative frequency output pressure sensor with single SOI NMOSFET suspended transducer. , 2011, , .		1
319	Hadrontherapy beam monitoring: Towards a new generation of ultra-thin p-type silicon strip detectors. , 2011, , .		3
320	Disruptive ultra-low-leakage design techniques for ultra-low-power mixed-signal microsystems. , 2011, , .		1
321	High-temperature perspectives of UTB SOI MOSFETs. , 2011, , .		3
322	CMOS test circuit architecture for the extraction of fluid properties using interdigitated electrodes microsensors. , 2011, , .		0
323	Contribution of carrier tunneling and gate induced drain leakage effects to the gate and drain currents of fin-shaped field-effect transistors. Journal of Applied Physics, 2011, 109, .	1.1	15
324	Effects of High-Energy Neutrons on Advanced SOI MOSFETs. Advanced Materials Research, 2011, 276, 95-105.	0.3	2

#	ARTICLE	IF	CITATIONS
325	Routes towards Novel Active Pressure Sensors in SOI Technology. <i>Advanced Materials Research</i> , 2011, 276, 145-155.	0.3	0
326	Performance of Ultra-Low-Power SOI CMOS Diodes Operating at Low Temperatures. <i>ECS Transactions</i> , 2011, 35, 325-330.	0.3	1
327	Ultra Low Power 3-D Flow Meter in Monolithic SOI Technology. <i>ECS Transactions</i> , 2011, 35, 319-324.	0.3	1
328	Transport-Confined Multi-Barrier FETs: A New Paradigm for Low-Leakage High On-Current Transistors. <i>ECS Transactions</i> , 2011, 35, 295-300.	0.3	0
329	Low temperature tunneling current enhancement in silicide/Si Schottky contacts with nanoscale barrier width. <i>Applied Physics Letters</i> , 2011, 98, .	1.5	7
330	Special Features of the Back-Gate Effects in Ultra-Thin Body SOI MOSFETs. <i>Engineering Materials</i> , 2011, , 323-339.	0.3	17
331	A Formal Study of Power Variability Issues and Side-Channel Attacks for Nanoscale Devices. <i>Lecture Notes in Computer Science</i> , 2011, , 109-128.	1.0	101
332	Information Theoretic and Security Analysis of a 65-Nanometer DDSLL AES S-Box. <i>Lecture Notes in Computer Science</i> , 2011, , 223-239.	1.0	25
333	Temperature and Silicon Film Thickness Influence on the Operation of Lateral SOI PIN Photodiodes for Detection of Short Wavelengths. <i>Journal of Integrated Circuits and Systems</i> , 2011, 6, 107-113.	0.3	10
334	Ultra low power CMOS circuits working in subthreshold regime for high temperature and radiation environments. <i>Additional Conferences (Device Packaging HiTEC HiTEN & CICMT)</i> , 2011, 2011, 000243-000250.	0.2	2
335	Gate Modulated Resonant Tunneling Transistor (RT-FET): Performance Investigation of a Steep Slope, High On-Current Device Through 3D Non-Equilibrium Green Function Simulations. <i>Engineering Materials</i> , 2011, , 201-214.	0.3	0
336	Sensing and MEMS Devices in Thin-Film SOI MOS Technology. <i>Engineering Materials</i> , 2011, , 355-392.	0.3	3
337	Implementation of the symmetric doped double-gate MOSFET model in Verilog- π A for circuit simulation. <i>International Journal of Numerical Modelling: Electronic Networks, Devices and Fields</i> , 2010, 23, 88-106.	1.2	15
338	Effect of high-energy neutrons on MuGFETs. <i>Solid-State Electronics</i> , 2010, 54, 196-204.	0.8	7
339	Substrate impact on threshold voltage and subthreshold slope of sub-32 nm ultra thin SOI MOSFETs with thin buried oxide and undoped channel. <i>Solid-State Electronics</i> , 2010, 54, 213-219.	0.8	42
340	Fully integrated blue/UV SOI CMOS photosensor for biomedical and environmental applications. <i>Analog Integrated Circuits and Signal Processing</i> , 2010, 65, 399-405.	0.9	10
341	Ultra low power flow-to-frequency SOI MEMS transducer. <i>Procedia Engineering</i> , 2010, 5, 540-543.	1.2	0
342	A fast and robust algorithm to assess respiratory frequency in real-time. <i>Procedia Engineering</i> , 2010, 5, 576-579.	1.2	2

#	ARTICLE	IF	CITATIONS
343	Compact model for single event transients and total dose effects at high temperatures for partially depleted SOI MOSFETs. <i>Microelectronics Reliability</i> , 2010, 50, 1852-1856.	0.9	21
344	Dynamic body potential variation in FD SOI MOSFETs operated in deep non-equilibrium regime: Model and applications. <i>Solid-State Electronics</i> , 2010, 54, 104-114.	0.8	22
345	Experimental study of transconductance and mobility behaviors in ultra-thin SOI MOSFETs with standard and thin buried oxides. <i>Solid-State Electronics</i> , 2010, 54, 164-170.	0.8	34
346	Study of Neutron Irradiation Effects on SOI and Strained SOI MuGFETs Assessed by Low-Frequency Noise. <i>ECS Transactions</i> , 2010, 31, 43-50.	0.3	3
347	Analysis of Lateral SOI PIN Diodes for the Detection of Blue and UV Wavelengths in a Wide Temperature Range. <i>ECS Transactions</i> , 2010, 31, 199-206.	0.3	6
348	Miniaturized and low cost innovative detection systems for medical and environmental applications. , 2010, , .		2
349	3D Simulation of Triple-Gate MOSFETs. , 2010, , .		2
350	Breaching the kT/q limit with dopant segregated Schottky barrier resonant tunneling MOSFETs: A computational study. , 2010, , .		1
351	Robustness-aware sleep transistor engineering for power-gated nanometer subthreshold circuits. , 2010, , .		6
352	Modeling of main leakage currents and their contribution to channel current in Fin-FETs. , 2010, , .		0
353	Parameter Extraction in Quadratic Exponential Junction Model with Series Resistance using Global Lateral Fitting. <i>ECS Transactions</i> , 2010, 31, 369-376.	0.3	7
354	Nanometer MOSFET Effects on the Minimum-Energy Point of Sub-45nm Subthreshold Logic--Mitigation at Technology and Circuit Levels. <i>ACM Transactions on Design Automation of Electronic Systems</i> , 2010, 16, 1-26.	1.9	6
355	An ultra-low-power frequency-tunable UWB pulse generator using 65nm CMOS technology. , 2010, , .		3
356	Miniaturized Wireless Sensing System for Real-Time Breath Activity Recording. <i>IEEE Sensors Journal</i> , 2010, 10, 178-184.	2.4	33
357	Ultra low power, harsh environment SOI-CMOS design of temperature sensor based threshold detection and wake-up IC. , 2010, , .		5
358	Glitch-induced within-die variations of dynamic energy in voltage-scaled nano-CMOS circuits. , 2010, , .		6
359	ULPFA: A New Efficient Design of a Power-Aware Full Adder. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2010, 57, 2066-2074.	3.5	103
360	I_{th}/I_{d} Method for Threshold Voltage Extraction Applicable in Advanced MOSFETs With Nonlinear Behavior Above Threshold. <i>IEEE Electron Device Letters</i> , 2010, 31, 930-932.	2.2	71

#	ARTICLE	IF	CITATIONS
361	Comparison between the behavior of submicron graded-channel SOI nMOSFETs with fully- and partially-depleted operations in a wide temperature range. , 2010, , .		2
362	An extended CAD methodology for sizing low-power low-voltage OTA architectures in decananometric technologies. , 2010, , .		0
363	Total-Dose Effects Caused by High-Energy Neutrons and γ -Rays in Multiple-Gate FETs. IEEE Transactions on Nuclear Science, 2010, 57, 1764-1770.	1.2	14
364	Testbed for IR-UWB based ranging and positioning: Experimental performance and comparison to CRLBs. , 2010, , .		7
365	Electrical characterization of SOI solar cells in a wide temperature range. , 2010, , .		1
366	Disruptive ultra-low-power SOI CMOS circuits towards μ W medical sensor implants. , 2010, , .		3
367	Complete microsystem using SOI photodiode for DNA concentration measurement. , 2010, , .		3
368	The detrimental impact of negative Celsius temperature on ultra-low-voltage CMOS logic. , 2010, , .		15
369	Thin-Film Lateral SOI PIN Diodes for Thermal Sensing Reaching the Cryogenic Regime. Journal of Integrated Circuits and Systems, 2010, 5, 160-167.	0.3	14
370	Compact modeling of the high temperature effect on the single event transient current generated by heavy ions in SOI 6T-SRAM. Additional Conferences (Device Packaging HiTEC HiTEN & CICMT), 2010, 2010, 000077-000082.	0.2	6
371	An electrical evaluation method for the silicidation of silicon nanowires. Applied Physics Letters, 2009, 95, 023106.	1.5	8
372	Comparison of ultra-low-power and static CMOS full adders in 0.15 μ m FD SOI CMOS. , 2009, , .		0
373	Impact of neutron irradiation on oxidized high-resistivity silicon substrates with and without a trap-rich passivation layer. , 2009, , .		2
374	Thermal sensing performance of lateral SOI PIN diodes in the 90–400 K range. , 2009, , .		5
375	Scaling trends of the AES S-box low power consumption in 130 and 65 nm CMOS technology nodes. , 2009, , .		15
376	Ultra-low-power high-noise-margin logic with undoped FD SOI devices. , 2009, , .		3
377	TRAPPIST Pixel Sensor with 2 μ m SOI technology. , 2009, , .		2
378	Optimization of Blue/UV Sensors Using PIN Photodiodes in Thin-Film SOI Technology. ECS Transactions, 2009, 19, 175-180.	0.3	14

#	ARTICLE	IF	CITATIONS
379	Floating-Body SOI Memory: Concepts, Physics and Challenges. ECS Transactions, 2009, 19, 243-256.	0.3	19
380	Nanometer MOSFET effects on the minimum-energy point of 45nm subthreshold logic. , 2009, , .		30
381	Technology flavor selection and adaptive techniques for timing-constrained 45nm subthreshold circuits. , 2009, , .		36
382	Mechanical properties of anodic aluminum oxide for microelectromechanical system applications. Journal of Vacuum Science & Technology B, 2009, 27, 542.	1.3	3
383	Analytical Modeling of Double Gate Graded-Channel SOI Transistors for Analog Applications. ECS Transactions, 2009, 19, 139-144.	0.3	0
384	On the Performance of Thin-Film Lateral SOI PIN Diodes as Thermal Sensors in a Wide Temperature Range. ECS Transactions, 2009, 23, 397-404.	0.3	3
385	Performance of Common-Source, Cascode and Wilson Current Mirrors Implemented with Graded-Channel SOI nMOSFETs in a Wide Temperature Range. ECS Transactions, 2009, 19, 265-270.	0.3	1
386	CMOS Compatible Anodic Al ₂ O ₃ Based Sensors for Bacteria Detection. Procedia Chemistry, 2009, 1, 1283-1286.	0.7	7
387	Analysis of source-follower buffers implemented with graded-channel SOI nMOSFETs operating at cryogenic temperatures. Cryogenics, 2009, 49, 599-604.	0.9	5
388	Direct protein detection with a nano-interdigitated array gate MOSFET. Biosensors and Bioelectronics, 2009, 24, 3531-3537.	5.3	40
389	Low power pulse generator as a capacitive interface for MEMS applications. , 2009, , .		3
390	A very high efficiency ultra-low-power 13.56MHz voltage rectifier in 150nm SOI CMOS. , 2009, , .		9
391	Interests and Limitations of Technology Scaling for Subthreshold Logic. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 1508-1519.	2.1	132
392	Drain / substrate coupling impact on DIBL of Ultra Thin Body and BOX SOI MOSFETs with undoped channel. , 2009, , .		6
393	High-efficiency solar cell embedded in SOI substrate for ULP autonomous circuits. , 2009, , .		16
394	A Simple Method for Measuring Si-Fin Sidewall Roughness by AFM. IEEE Nanotechnology Magazine, 2009, 8, 611-616.	1.1	23
395	Total-dose effects caused by high-energy neutrons and γ -rays in Multiple-Gate FETs. , 2009, , .		3
396	Enhanced performance of SERDES current-mode output driver using 0.13 μ m PD SOI CMOS. , 2009, , .		1

#	ARTICLE	IF	CITATIONS
397	Efficient single event upset simulations of a tolerant PD SOI CMOS D Flip-Flop. , 2009, , .		4
398	Fluid characterization by interdigitated electrodes sensors. IFMBE Proceedings, 2009, , 2396-2399.	0.2	0
399	Study and implementation of a wireless accelerometer network for gait analysis. IFMBE Proceedings, 2009, , 2073-2076.	0.2	3
400	Bio-compatible Insulated Substrate Impedance Transducers. IFMBE Proceedings, 2009, , 1180-1183.	0.2	0
401	Wireless microsensors system for monitoring breathing activity. IFMBE Proceedings, 2009, , 875-879.	0.2	1
402	Low-cost miniaturized UV photosensor for direct measurement of DNA concentration within a closed tube container. IFMBE Proceedings, 2009, , 1057-1061.	0.2	3
403	Harmonic distortion analysis of double gate graded-channel MOSFETs operating in saturation. Microelectronics Journal, 2008, 39, 1663-1670.	1.1	26
404	Building ultra-low-power high-temperature digital circuits in standard high-performance SOI technology. Solid-State Electronics, 2008, 52, 1939-1945.	0.8	11
405	Advantages of graded-channel SOI nMOSFETs for application as source-follower analog buffer. Solid-State Electronics, 2008, 52, 1933-1938.	0.8	10
406	Silicon-on-Nothing MOSFETs: An efficient solution for parasitic substrate coupling suppression in SOI devices. Applied Surface Science, 2008, 254, 6168-6173.	3.1	22
407	NANOSIL network of excellence"silicon-based nanostructures and nanodevices for long-term nanoelectronics applications. Materials Science in Semiconductor Processing, 2008, 11, 148-159.	1.9	1
408	Carrier Mobility in Undoped Triple-Gate FinFET Structures and Limitations of Its Description in Terms of Top and Sidewall Channel Mobilities. IEEE Transactions on Electron Devices, 2008, 55, 3532-3541.	1.6	37
409	Analysis and minimization of practical energy in 45nm subthreshold logic circuits. , 2008, , .		24
410	Sub-45nm fully-depleted SOI CMOS subthreshold logic for ultra-low-power applications. , 2008, , .		11
411	Very High Efficiency 13.56 MHz RFID Input Stage Voltage Multipliers Based On Ultra Low Power MOS Diodes. , 2008, , .		9
412	Systematic HDL Design of a S-? Fractional-N Phase-Locked Loop for Wireless Applications. , 2008, , .		0
413	Linearity Analysis in Double Gate Graded-Channel Soi Devices Applied to 2-Mos Mosfet-C Balanced Structures. ECS Transactions, 2008, 14, 273-282.	0.3	1
414	Channel Length Influence on the Performance of Source-Follower Buffers Implemented with Graded-Channel SOI nMOSFETs. ECS Transactions, 2008, 14, 263-272.	0.3	1

#	ARTICLE	IF	CITATIONS
415	Characterization of ultrathin SOI film and application to short channel MOSFETs. Nanotechnology, 2008, 19, 165703.	1.3	15
416	A Capacitorless 1T-DRAM on SOI Based on Dynamic Coupling and Double-Gate Operation. IEEE Electron Device Letters, 2008, 29, 795-798.	2.2	87
417	Impact of Technology Scaling on Digital Subthreshold Circuits. , 2008, , .		12
418	Low-power dihexylquaterthiophene-based thin film transistors for analog applications. Applied Physics Letters, 2008, 92, .	1.5	7
419	Impact of layout style and parasitic capacitances in full adder. , 2008, , .		0
420	Study of Matching Properties of Graded-Channel SOI MOSFETs. Journal of Integrated Circuits and Systems, 2008, 3, 69-75.	0.3	8
421	The Length-Dependence of the 1/f Noise of Graded-Channel SOI nMOSFETs. ECS Transactions, 2007, 9, 373-381.	0.3	1
422	Notice of Violation of IEEE Publication Principles HDL system-level design of O-QPSK receiver for 2.4-GHz band IEEE 802.15.4. , 2007, , .		0
423	Wide-Band Simulation and Characterization of Digital Substrate Noise in SOI Technology. , 2007, , .		2
424	Building Ultra-Low-Power Low-Frequency Digital Circuits with High-Speed Devices. , 2007, , .		18
425	Impact of Graded-Channel SOI MOSFET Application on the Performance of Cascode and Wilson Current Mirrors. ECS Transactions, 2007, 9, 441-450.	0.3	4
426	Channel Length Reduction Influence on Harmonic Distortion of Graded-Channel Gate-All-Around Devices. ECS Transactions, 2007, 4, 247-256.	0.3	2
427	Analysis of Matching in Graded-Channel SOI MOSFETs. ECS Transactions, 2007, 9, 323-332.	0.3	2
428	Improved Charge Sheet Model for PD SOI Sub-Micron MOSFETs. ECS Transactions, 2007, 9, 451-459.	0.3	1
429	Application of Double Gate Graded-Channel SOI in MOSFET-C Balanced Structures. ECS Transactions, 2007, 6, 217-222.	0.3	2
430	Low Leakage SOI CMOS Static Memory Cell With Ultra-Low Power Diode. IEEE Journal of Solid-State Circuits, 2007, 42, 689-702.	3.5	29
431	A CMOS High-Q LC Eight-Path Bandpass Filter for Wireless Broadband Applications. , 2007, , .		0
432	System-Level Analysis of O-QPSK Transceiver for 2.4-GHZ Band IEEE 802.15.4 Zigbee Standard. , 2007, , .		7

#	ARTICLE	IF	CITATIONS
433	Experiments and Modeling of Dynamic Floating Body Effects in 1T-Dram Fully Depleted SOI Devices. , 2007, , .		2
434	Substrate Bias Effect Linked to Parasitic Series Resistance in Multiple-Gate SOI MOSFETs. IEEE Electron Device Letters, 2007, 28, 834-836.	2.2	20
435	A SOI CMOS Smart High-Temperature Sensor. SOI Conference, Proceedings of the IEEE International, 2007, , .	0.0	9
436	SOI Devices and Ring Oscillators on Thin Dielectric Membranes For Pressure Sensing Applications. SOI Conference, Proceedings of the IEEE International, 2007, , .	0.0	1
437	On the Origin of the Excess Low-Frequency Noise in Graded-Channel Silicon-on-Insulator nMOSFETs. IEEE Electron Device Letters, 2007, 28, 919-921.	2.2	4
438	Frequency Variation of the Small-Signal Output Conductance of Decanometer MOSFETs Due to Substrate Crosstalk. IEEE Electron Device Letters, 2007, 28, 419-421.	2.2	24
439	Fully Integrated High-Q Switched Capacitor Bandpass Filter with Center Frequency and Bandwidth Tuning. Radio Frequency Integrated Circuits (RFIC) Symposium, IEEE, 2007, , .	0.0	36
440	The low-frequency noise behaviour of graded-channel SOI nMOSFETs. Solid-State Electronics, 2007, 51, 260-267.	0.8	12
441	Thin film fully-depleted SOI four-gate transistors. Solid-State Electronics, 2007, 51, 278-284.	0.8	22
442	Planar double-gate SOI MOS devices: Fabrication by wafer bonding over pre-patterned cavities and electrical characterization. Solid-State Electronics, 2007, 51, 231-238.	0.8	34
443	Compact model for highly-doped double-gate SOI MOSFETs targeting baseband analog applications. Solid-State Electronics, 2007, 51, 655-661.	0.8	54
444	Innovating SOI memory devices based on floating-body effects. Solid-State Electronics, 2007, 51, 1252-1262.	0.8	40
445	Electrical characterization of true Silicon-On-Nothing MOSFETs fabricated by Si layer transfer over a pre-etched cavity. Solid-State Electronics, 2007, 51, 1238-1244.	0.8	32
446	Reduction of gate-to-channel tunneling current in FinFET structures. Solid-State Electronics, 2007, 51, 1466-1472.	0.8	17
447	Dynamic differential self-timed logic families for robust and low-power security ICs. The Integration VLSI Journal, 2007, 40, 355-364.	1.3	12
448	Electrical detection of DNA hybridization: Three extraction techniques based on interdigitated Al/Al ₂ O ₃ capacitors. Biosensors and Bioelectronics, 2007, 22, 2199-2207.	5.3	66
449	Harmonic distortion analysis using an improved charge sheet model for PD SOI MOSFETs. Microelectronics Journal, 2007, 38, 321-326.	1.1	4
450	The meta-stable dip (MSD) effect in SOI FinFETs. Microelectronic Engineering, 2007, 84, 590-593.	1.1	2

#	ARTICLE	IF	CITATIONS
451	A 3-D Analytical Physically Based Model for the Subthreshold Swing in Undoped Trigate FinFETs. IEEE Transactions on Electron Devices, 2007, 54, 2487-2496.	1.6	56
452	Bulk and surface micromachined MEMS in thin film SOI technology. Electrochimica Acta, 2007, 52, 2850-2861.	2.6	16
453	Characterization of quantum efficiency, effective lifetime and mobility in thin film ungated SOI lateral PIN photodiodes. Solid-State Electronics, 2007, 51, 337-342.	0.8	26
454	Specific features of multiple-gate MOSFET threshold voltage and subthreshold slope behavior at high temperatures. Solid-State Electronics, 2007, 51, 1185-1193.	0.8	26
455	Characterization of FD SOI devices and VCOs on thin dielectric membranes under pressure. Solid-State Electronics, 2007, 51, 1229-1237.	0.8	14
456	Electrical Characterization and Special Properties of FINFET Structures. NATO Science for Peace and Security Series B: Physics and Biophysics, 2007, , 199-220.	0.2	4
457	Substrate Effect on the Output Conductance Frequency Response of SOI MOSFETs. NATO Science for Peace and Security Series B: Physics and Biophysics, 2007, , 221-238.	0.2	4
458	Nonlinearity Analysis of FinFETs. , 2006, , .		4
459	Experimental Evidence for Reduction of Gate Tunneling Current in FinFET Structures and Its Dependence on the Fin Width. Solid-State Device Research Conference, 2008 ESSDERC 2008 38th European, 2006, , .	0.0	4
460	Speed performances of thin-film lateral SOI PIN photodiodes up to tens of GHz. SOI Conference, Proceedings of the IEEE International, 2006, , .	0.0	7
461	On-Chip RF Detection of DNA Hybridization Based on Interdigitated Al/Al ₂ O ₃ Capacitors. Solid-State Device Research Conference, 2008 ESSDERC 2008 38th European, 2006, , .	0.0	1
462	Abnormal drain current (ADC) effect and its mechanism in FD SOI MOSFETs. IEEE Electron Device Letters, 2006, 27, 123-126.	2.2	4
463	Cryogenic operation of graded-channel silicon-on-insulator nMOSFETs for high performance analog applications. Microelectronics Journal, 2006, 37, 137-144.	1.1	4
464	Gain improvement in operational transconductance amplifiers using Graded-Channel SOI nMOSFETS. Microelectronics Journal, 2006, 37, 31-37.	1.1	12
465	Low-swing current mode logic (LSCML): A new logic style for secure and robust smart cards against power analysis attacks. Microelectronics Journal, 2006, 37, 997-1006.	1.1	20
466	Continuous high-temperature model for low-doped accumulation mode silicon-on-insulator pMOSFETs. Solid-State Electronics, 2006, 50, 1261-1268.	0.8	0
467	Self-cascode SOI versus graded-channel SOI MOS transistors. IET Circuits, Devices and Systems, 2006, 153, 461.	0.6	21
468	Characterization and design methodology for low-distortion MOSFET-C analog structures in multithreshold deep-submicrometer SOI CMOS technologies. IEEE Transactions on Electron Devices, 2006, 53, 263-269.	1.6	9

#	ARTICLE	IF	CITATIONS
469	Analog/RF performance of multiple gate SOI devices: wideband simulations and characterization. IEEE Transactions on Electron Devices, 2006, 53, 1088-1095.	1.6	156
470	Monolithically integrated 10â€¦Gbit/s photodiode and transimpedance amplifier in thin-film SOI CMOS technology. Electronics Letters, 2006, 42, 1420.	0.5	10
471	Low-Voltage Low-Power High-Temperature SOI CMOS Rectifiers. SOI Conference, Proceedings of the IEEE International, 2006, , .	0.0	6
472	Impact of Asymmetric Channel Configuration on the Linearity of Double-Gate SOI MOSFETs. , 2006, , .		4
473	Novel Capacitor-Less 1T-DRAM Using MSD Effect. SOI Conference, Proceedings of the IEEE International, 2006, , .	0.0	5
474	CLOCK JITTER EFFECT ON SWITCHED-CAPACITOR FILTER DESIGN. Fluctuation and Noise Letters, 2006, 06, L29-L33.	1.0	1
475	Analysis of quasi double gate method for performance prediction of deep submicron double gate SOI MOSFETs. Semiconductor Science and Technology, 2005, 20, 423-429.	1.0	25
476	High frequency degradation of body-contacted PD SOI MOSFET output conductance. Semiconductor Science and Technology, 2005, 20, 469-472.	1.0	14
477	Effective mobility in FinFET structures with HfO2 and SiON gate dielectrics and TaN gate electrode. Microelectronic Engineering, 2005, 80, 386-389.	1.1	44
478	On the great potential of non-doped MOSFETs for analog applications in partially-depleted SOI CMOS process. Solid-State Electronics, 2005, 49, 708-715.	0.8	13
479	A new multi-valued current-mode adder based on negative-differential resistance using ULP diodes. Solid-State Electronics, 2005, 49, 1185-1191.	0.8	2
480	FinFET analogue characterization from DC to 110GHz. Solid-State Electronics, 2005, 49, 1488-1496.	0.8	142
481	A new memory effect (MSD) in fully depleted SOI MOSFETs. Solid-State Electronics, 2005, 49, 1547-1555.	0.8	50
482	A charge-based continuous model for submicron graded-channel nMOSFET for analog circuit simulation. Solid-State Electronics, 2005, 49, 1683-1692.	0.8	10
483	High performance analog operation of double gate transistors with the graded-channel architecture at low temperatures. Solid-State Electronics, 2005, 49, 1569-1575.	0.8	14
484	Advantages of the Graded-Channel SOI FD MOSFET for Application as a Quasi-Linear Resistor. IEEE Transactions on Electron Devices, 2005, 52, 967-972.	1.6	32
485	Physical Modeling and Design of Thin-Film SOI Lateral PIN Photodiodes. IEEE Transactions on Electron Devices, 2005, 52, 1116-1122.	1.6	61
486	SOI-CMOS compatible low-power gas sensor using sputtered and drop-coated metal-oxide active layers. Microsystem Technologies, 2005, 12, 160-168.	1.2	12

#	ARTICLE	IF	CITATIONS
487	Low Temperature and Channel Engineering Influence on Harmonic Distortion of SOI nMOSFETs for Analog Applications. ECS Meeting Abstracts, 2005, , .	0.0	2
488	Comparison of DNA detection methods using nanoparticles and silver enhancement. IET Nanobiotechnology, 2005, 152, 3.	2.1	15
489	A revised reverse gated-diode technique for determining generation parameters in thin-film silicon-on-insulator devices and its application at high temperatures. Journal of Applied Physics, 2005, 97, 093718.	1.1	13
490	Accurate effective mobility extraction by split C-V technique in SOI MOSFETs: suppression of the influence of floating-body effects. IEEE Electron Device Letters, 2005, 26, 749-751.	2.2	22
491	Recent Advances in SOI MOSFET Devices and Circuits for Ultra-Low Power / High Temperature Applications. , 2005, , 133-144.		1
492	Radiation Effect on Electrical Properties of Fully-Depleted Unibond SOI MOSFETs. , 2005, , 233-239.		0
493	Characterization of Carrier Generation in Thin-Film SOI Devices by Reverse Gated-Diode Technique and its Application at High Temperatures. , 2005, , 247-254.		1
494	LOW-NOISE SILICON-ON-INSULATOR HALL DEVICES. Fluctuation and Noise Letters, 2004, 04, L345-L354.	1.0	3
495	Sensitive DNA electrical detection based on interdigitated Al/Al ₂ O ₃ microelectrodes. Sensors and Actuators B: Chemical, 2004, 98, 269-274.	4.0	76
496	Determination of film and surface recombination in thin-film SOI devices using gated-diode technique. Solid-State Electronics, 2004, 48, 389-399.	0.8	23
497	Laterally asymmetric channel engineering in fully depleted double gate SOI MOSFETs for high performance analog applications. Solid-State Electronics, 2004, 48, 947-959.	0.8	95
498	Composite ULP diode fabrication, modelling and applications in multi-V _{th} FD SOI CMOS technology. Solid-State Electronics, 2004, 48, 1017-1025.	0.8	47
499	Integral function method for determination of nonlinear harmonic distortion. Solid-State Electronics, 2004, 48, 2225-2234.	0.8	59
500	LDMOS in SOI technology with very-thin silicon film. Solid-State Electronics, 2004, 48, 2263-2270.	0.8	54
501	Thin films stress extraction using micromachined structures and wafer curvature measurements. Microelectronic Engineering, 2004, 76, 219-226.	1.1	73
502	AC Behavior of Gate-Induced Floating Body Effects in Ultrathin Oxide PD SOI MOSFETs. IEEE Electron Device Letters, 2004, 25, 104-106.	2.2	12
503	Power-delay product minimization in high-performance 64-bit carry-select adders. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2004, 12, 235-244.	2.1	36
504	SOI CMOS Compatible Low-Power Microheater Optimization for the Fabrication of Smart Gas Sensors. IEEE Sensors Journal, 2004, 4, 670-680.	2.4	58

#	ARTICLE	IF	CITATIONS
505	Low Power Analog CMOS for Cardiac Pacemakers. , 2004, , .		25
506	SOI Technology for Single-Chip Harsh Environment Microsystems. , 2004, , .		1
507	Investigation of Low-Power Low-Voltage Circuit Techniques for a Hybrid Full-Adder Cell. Lecture Notes in Computer Science, 2004, , 189-197.	1.0	5
508	Soi Technology. , 2004, , 49-64.		0
509	Modeling of the bulk versus SOI CMOS performances for the optimal design of APS circuits in low-power low-voltage applications. IEEE Transactions on Electron Devices, 2003, 50, 106-110.	1.6	14
510	FD MOS SOI circuit to enhance the ratio of illuminated to dark current of a co-integrated a-Si:H photodiode. Microelectronics Reliability, 2003, 43, 189-193.	0.9	3
511	A review of leakage current in SOI CMOS ICs: impact on parametric testing techniques. Solid-State Electronics, 2003, 47, 1959-1967.	0.8	5
512	Immobilization of DNA on CMOS compatible materials. Sensors and Actuators B: Chemical, 2003, 92, 90-97.	4.0	35
513	Influence of device engineering on the analog and RF performances of SOI MOSFETs. IEEE Transactions on Electron Devices, 2003, 50, 577-588.	1.6	195
514	SOI technology for future high-performance smart cards. IEEE Micro, 2003, 23, 58-67.	1.8	2
515	Floating effective back-gate effect on the small-signal output conductance of SOI MOSFETs. IEEE Electron Device Letters, 2003, 24, 414-416.	2.2	45
516	Low-noise SOI Hall devices. , 2003, , .		8
517	Substrate Effects on the Small-Signal Characteristics of SOI MOSFETs. , 2002, , .		8
518	SOI CMOS TRANSISTORS FOR RF AND MICROWAVE APPLICATIONS. Selected Topics in Electornics and Systems, 2002, , 273-362.	0.2	4
519	25 to 300Â°C ultra-low-power voltage reference compatible with standard SOI CMOS process. Electronics Letters, 2002, 38, 1103.	0.5	10
520	Low temperature operation of graded-channel SOI nMOSFETs for analog applications. , 2002, , .		0
521	<title>Fully CMOS-compatible low-power microheater</title>. , 2002, , .		5
522	A modified Bosch-type process for precise surface micromachining of polysilicon. Journal of Micromechanics and Microengineering, 2002, 12, 328-333.	1.5	12

#	ARTICLE	IF	CITATIONS
523	Influence of HALO implantation on analog performance and comparison between bulk, partially-depleted and fully-depleted MOSFETs. , 2002, , .		4
524	On the high-temperature subthreshold slope of thin-film SOI MOSFETs. IEEE Electron Device Letters, 2002, 23, 148-150.	2.2	27
525	A method to extract mobility degradation and total series resistance of fully-depleted SOI MOSFETs. IEEE Transactions on Electron Devices, 2002, 49, 82-88.	1.6	19
526	SOI n-MOSFET low-frequency noise measurements and modeling from room temperature up to 250°C. IEEE Transactions on Electron Devices, 2002, 49, 1289-1295.	1.6	28
527	0.25 μm fully depleted SOI MOSFETs for RF mixed analog-digital circuits, including a comparison with partially depleted devices with relation to high frequency noise parameters. Solid-State Electronics, 2002, 46, 379-386.	0.8	20
528	New method for determination of harmonic distortion in SOI FD transistors. Solid-State Electronics, 2002, 46, 103-108.	0.8	51
529	Analog circuit design using graded-channel silicon-on-insulator nMOSFETs. Solid-State Electronics, 2002, 46, 1215-1225.	0.8	33
530	Analysis of the thin-film SOI lateral bipolar transistor and optimization of its output characteristics for high-temperature applications. Solid-State Electronics, 2002, 46, 1339-1343.	0.8	7
531	Low-Noise High-Temperature SOI Analog Circuits. , 2002, , 189-209.		3
532	Low temperature operation of graded-channel SOI nMOSFETs for analog applications. European Physical Journal Special Topics, 2002, 12, 23-26.	0.2	4
533	Design of a Branch-Based Carry-Select Adder IP Portable in 0.25 μm Bulk and Silicon-On-Insulator CMOS Technologies. IFIP Advances in Information and Communication Technology, 2002, , 169-180.	0.5	0
534	Integrated sensor and electronic circuits in fully depleted SOI technology for high-temperature applications. IEEE Transactions on Industrial Electronics, 2001, 48, 272-280.	5.2	19
535	Investigation of Deep Submicron Single and Double Gate SOI MOSFETs in Accumulation Mode for Enhanced Performance. Electrochemical and Solid-State Letters, 2001, 4, G28.	2.2	20
536	Fully depleted SOI CMOS technology for heterogeneous micropower, high-temperature or RF microsystems. Solid-State Electronics, 2001, 45, 541-549.	0.8	81
537	Hall effect measurements in double-gate SOI MOSFETs. Solid-State Electronics, 2001, 45, 1793-1798.	0.8	11
538	Deep-submicrometer DC-to-RF SOI MOSFET macro-model. IEEE Transactions on Electron Devices, 2001, 48, 1981-1988.	1.6	5
539	Total-dose effects in double-gate-controlled NPN bipolar transistors. IEEE Transactions on Nuclear Science, 2001, 48, 1694-1699.	1.2	0
540	SOI CMOS TRANSISTORS FOR RF AND MICROWAVE APPLICATIONS. International Journal of High Speed Electronics and Systems, 2001, 11, 1159-1248.	0.3	23

#	ARTICLE	IF	CITATIONS
541	Graded-channel fully depleted Silicon-On-Insulator nMOSFET for reducing the parasitic bipolar effects. Solid-State Electronics, 2000, 44, 917-922.	0.8	56
542	Analog performance and application of graded-channel fully depleted SOI MOSFETs. Solid-State Electronics, 2000, 44, 1219-1222.	0.8	67
543	New experiments on the electrodeposition of iron in porous silicon. Microelectronics Reliability, 2000, 40, 877-879.	0.9	19
544	Process alternative: SOI for heterogeneous systems. Microelectronic Engineering, 2000, 54, 49-62.	1.1	0
545	Investigation of single and double gate SOI MOSFETs in Accumulation Mode for enhanced performances and reduced technological drawbacks. , 2000, , .		2
546	High-temperature sigma-delta modulator in thin-film fully-depleted SOI technology. Electronics Letters, 1999, 35, 749.	0.5	10
547	Gate-all-around OTA's for rad-hard and high-temperature analog applications. IEEE Transactions on Nuclear Science, 1999, 46, 1242-1249.	1.2	20
548	Title is missing!. Analog Integrated Circuits and Signal Processing, 1999, 21, 213-228.	0.9	54
549	A physically-based C/sub \hat{z} /-continuous model for accumulation-mode SOI pMOSFETs. IEEE Transactions on Electron Devices, 1999, 46, 2295-2303.	1.6	16
550	Carrier lifetime extraction in fully depleted dual-gate SOI devices. IEEE Electron Device Letters, 1999, 20, 209-211.	2.2	8
551	An Asymmetric Channel SOI nMOSFET for Reducing Parasitic Effects and Improving Output Characteristics. Electrochemical and Solid-State Letters, 1999, 3, 50.	2.2	32
552	Magnetic-field sensor based on a thin-film SOI transistor. Sensors and Actuators A: Physical, 1998, 67, 96-101.	2.0	9
553	Thin-film SOI n-MOSFET low-frequency noise measurements at elevated temperatures. , 1998, , .		8
554	Potential and modeling of 1- $\frac{1}{4}$ m SOI CMOS operational transconductance amplifiers for applications up to 1 GHz. IEEE Journal of Solid-State Circuits, 1998, 33, 640-643.	3.5	19
555	The Gm/ID Methodology on MATLAB: a pedagogical tool for analog integrated circuit design education. , 1998, , 109-112.		0
556	Comparison of TiSi ₂ , CoSi ₂ , and NiSi for Thin-Film Silicon-On-Insulator Applications. Journal of the Electrochemical Society, 1997, 144, 2437-2442.	1.3	102
557	Improved synthesis of gain-boosted regulated-cascode CMOS stages using symbolic analysis and gm/ID methodology. IEEE Journal of Solid-State Circuits, 1997, 32, 1006-1012.	3.5	76
558	Potential and modelling of 1 [micro sign]m 1 GHz SOI CMOS OTAs. Electronics Letters, 1997, 33, 774.	0.5	3

#	ARTICLE	IF	CITATIONS
559	Unified 1/f noise SOI MOSFET modelling for circuit simulation. Electronics Letters, 1997, 33, 1781.	0.5	2
560	Substrate crosstalk reduction using SOI technology. IEEE Transactions on Electron Devices, 1997, 44, 2252-2261.	1.6	251
561	Fully depleted SOI-CMOS technology for high temperature IC applications. Materials Science and Engineering B: Solid-State Materials for Advanced Technology, 1997, 46, 1-7.	1.7	19
562	Comparison of self-heating effect in GAA and SOI mosfets. Microelectronics Reliability, 1997, 37, 61-75.	0.9	5
563	A $g/m/D$ based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA. IEEE Journal of Solid-State Circuits, 1996, 31, 1314-1319.	3.5	534
564	Design of SOI CMOS operational amplifiers for applications up to 300°C. IEEE Journal of Solid-State Circuits, 1996, 31, 179-186.	3.5	98
565	Improvement of SOI MOS current-mirror performances using serial-parallel association of transistors. Electronics Letters, 1996, 32, 278.	0.5	10
566	A physically-based C_{eff} -continuous fully-depleted SOI MOSFET model for analog applications. IEEE Transactions on Electron Devices, 1996, 43, 568-575.	1.6	53
567	The effect of series resistance on threshold voltage measurement techniques for fully depleted SOI MOSFETs. Solid-State Electronics, 1996, 39, 89-94.	0.8	6
568	Modelling and application of fully depleted SOI MOSFETs for low voltage, low power analogue CMOS circuits. Solid-State Electronics, 1996, 39, 455-460.	0.8	62
569	Measurement and modeling of thin-film accumulation-mode SOI p-MOSFET intrinsic gate capacitances. Solid-State Electronics, 1996, 39, 1071-1078.	0.8	7
570	Measurement and two-dimensional simulation of thin-film SOI MOSFETs: Intrinsic gate capacitances at elevated temperatures. Solid-State Electronics, 1996, 39, 1613-1619.	0.8	5
571	Theoretical considerations for SRAM total-dose hardening. IEEE Transactions on Nuclear Science, 1995, 42, 83-91.	1.2	6
572	Silicon-on-insulator technology for high temperature metal oxide semiconductor devices and circuits. Materials Science and Engineering B: Solid-State Materials for Advanced Technology, 1995, 29, 7-12.	1.7	39
573	Moderate inversion model of ultrathin double-gate nMOS/SOI transistors. Solid-State Electronics, 1995, 38, 171-176.	0.8	31
574	Charge-sheet modelling of MOS I-V fundamental nonlinearities in MOSFET-C continuous-time filters. Electronics Letters, 1995, 31, 1419-1420.	0.5	22
575	P+-P-P+ pseudo-bipolar lateral SOI transistor. Electronics Letters, 1994, 30, 1543-1545.	0.5	3
576	Comparison of SOI versus bulk performances of CMOS micropower single-stage OTAs. Electronics Letters, 1994, 30, 1933-1934.	0.5	38

#	ARTICLE	IF	CITATIONS
577	Subthreshold slope of long-channel, accumulation-mode p-channel SOI MOSFETs. Solid-State Electronics, 1994, 37, 289-294.	0.8	50
578	Comments on "numerical analysis of small-signal characteristics of a fully depleted SOI MOSFET". Solid-State Electronics, 1994, 37, 1447-1448.	0.8	3
579	Modeling of ultrathin double-gate nMOS/SOI transistors. IEEE Transactions on Electron Devices, 1994, 41, 715-720.	1.6	140
580	Radiation-hard design for SOI MOS inverters. IEEE Transactions on Nuclear Science, 1994, 41, 402-407.	1.2	18
581	Latch and hot-electron gate current in accumulation-mode SOI p-MOSFET's. IEEE Electron Device Letters, 1994, 15, 157-159.	2.2	8
582	Kink-like effect in long n-channel twin-gate fully-depleted SOI MOSFETs. Electronics Letters, 1994, 30, 1456-1458.	0.5	1
583	Evidence of different conduction mechanisms in accumulation-mode p-channel SOI MOSFET's at room and liquid-helium temperatures. IEEE Transactions on Electron Devices, 1993, 40, 727-732.	1.6	24
584	Analysis of floating substrate effects on the intrinsic gate capacitance of SOI MOSFETs using two-dimensional device simulation. IEEE Transactions on Electron Devices, 1993, 40, 1789-1796.	1.6	21
585	Demonstration of the potential of accumulation-mode MOS transistors on SOI substrates for high-temperature operation (150-300 degrees C). IEEE Electron Device Letters, 1993, 14, 10-12.	2.2	47
586	Extraction of physical device dimensions of SOI MOSFETs from gate capacitance measurements. Electronics Letters, 1993, 29, 586.	0.5	4
587	Extended theoretical analysis of the steady-state linear behaviour of accumulation-mode, long-channel p-MOSFETs on SOI substrates. Solid-State Electronics, 1992, 35, 1085-1092.	0.8	29
588	Physics and performances of accumulation-mode SOI p-MOSFET's from low (77 K) to high (150-320°C) temperatures. Microelectronic Engineering, 1992, 19, 803-806.	1.1	0
589	Characteristics of nMOS/GAA (Gate-All-Around) transistors near threshold. Microelectronic Engineering, 1992, 19, 815-818.	1.1	18
590	Measurement and simulation of floating substrate effects on the intrinsic gate capacitance characteristics of SOI n-MOSFETs. Electronics Letters, 1992, 28, 967-969.	0.5	6
591	Measurement of threshold voltages of thin-film accumulation-mode PMOS/SOI transistors. IEEE Electron Device Letters, 1991, 12, 682-684.	2.2	84
592	Interpretation of quasi-static C-V characteristics of MOSOS capacitors on SOI substrates. Electronics Letters, 1991, 27, 43-44.	0.5	5
593	Problems in designing thin-film accumulation-mode p-channel SOI MOSFETs for CMOS digital circuit environment. Electronics Letters, 1991, 27, 1280.	0.5	10
594	ac capacitance and conductance measurements of two-terminal metal-oxide-semiconductor capacitors on silicon-insulator substrates. Journal of Applied Physics, 1991, 70, 5111-5113.	1.1	1

#	ARTICLE	IF	CITATIONS
595	Measurement of intrinsic gate capacitances of SOI MOSFET's. IEEE Electron Device Letters, 1990, 11, 291-293.	2.2	15
596	A Physical Model for the Characterization of SOI MOSFETs in Linear Operation. , 1989, , 755-758.		0
597	A new analytical model for the two-terminal MOS capacitor on SOI substrate. IEEE Electron Device Letters, 1988, 9, 296-299.	2.2	30
598	THEORETICAL ANALYSIS OF THE TWO-TERMINAL MOS CAPACITOR ON SOI SUBSTRATE. Journal De Physique Colloque, 1988, 49, C4-67-C4-70.	0.2	0
599	Thin-film fully-depleted SOI CMOS technology, devices and circuits for LVLP analog/digital/microwave applications. , 0, , .		1
600	Characterization of SOI MOSFETs by gate capacitance measurements. , 0, , .		2
601	Design Techniques for High-Speed Low-Power and High-Temperature Digital Cmos Circuits on Soi. , 0, , .		6
602	High Temperature Characteristics of Gaa/soi Transistors and Circuits. , 0, , .		2
603	Subthreshold slope of accumulation-mode p-channel SOI MOSFETs. , 0, , .		1
604	Comparison of hot-carrier effects in thin-film SOI and gate-all-around accumulation-mode p-MOSFETs. , 0, , .		1
605	Design and performance of a new flash EEPROM on SOI(SIMOX) substrates. , 0, , .		4
606	Design of thin-film fully-depleted SOI CMOS analog circuits significantly outperforming bulk implementations. , 0, , .		17
607	Potential of SOI for analog and mixed analog-digital low-power applications. , 0, , .		12
608	A comparative study of non-linearities in bulk and SOI linear resistors based on 2- and 4-transistor structures. , 0, , .		4
609	A 1-GHz operational transconductance amplifier in SOI technology. , 0, , .		5
610	Coupling effects in high-resistivity SIMOX substrates for VHF and microwave applications. , 0, , .		1
611	Extended study of crosstalk in SOI-SIMOX substrates. , 0, , .		28
612	A low-voltage, low-power microwave SOI MOSFET. , 0, , .		13

#	ARTICLE	IF	CITATIONS
613	A SOI-CMOS micro-power first-order sigma-delta modulator. , 0, , .		2
614	SOI implementation of low-voltage and high-temperature MOSFET-C continuous-time filters. , 0, , .		0
615	CAD-compatible model for accumulation-mode (AM) SOI pMOSFETs. , 0, , .		0
616	Comparison of charge injection in SOI and bulk MOS analog switches. , 0, , .		3
617	SOI current and voltage reference sources for applications up to 300Â°C. , 0, , .		6
618	High-temperature analog instrumentation system in thin-film fully-depleted SOI CMOS technology. , 0, , .		3
619	Advanced SOI CMOS technology for RF applications. , 0, , .		3
620	A bandgap circuit operating up to 300Â°C using lateral bipolar transistors in thin-film CMOS-SOI technology. , 0, , .		0
621	High-temperature characterization of a PD SOI CMOS process with LDMOS and lateral bipolar structures. , 0, , .		2
622	A bandgap circuit operating up to 300Â°C using lateral bipolar transistors in thin-film CMOS-SOI technology. , 0, , .		13
623	The art of high temperature FD-SOI CMOS. , 0, , .		3
624	Smart card circuits in SOI technology. , 0, , .		3
625	Analysis and design of a family of low-power class AB operational amplifiers. , 0, , .		5
626	Comparison of floating-body effects in conventional and graded-channel fully-depleted silicon-on-insulator nMOSFETs. , 0, , .		2
627	Comparison of 0.25 μ m bulk, PD and FD SOI CMOS implementations of a low-voltage low-power programmable DLL for linear delay generation. , 0, , .		3
628	Characterization, simulation and modeling of PLL under irradiation using HDL-A. , 0, , .		0
629	An efficient and accurate procedure to evaluate distortion in SOI FD MOSFET. , 0, , .		5
630	Analog circuit design using graded-channel SOI nMOSFETs. , 0, , .		3

#	ARTICLE	IF	CITATIONS
631	A procedure to extract mobility degradation, series resistance and threshold voltage of SOI MOSFETs in the saturation region. , 0, , .		4
632	IF MEMS filters for mobile communication. , 0, , .		3
633	SOI CMOS compatible low-power microheater optimization and fabrication for smart gas sensor implementations. , 0, , .		8
634	Intelligent SOI CMOS integrated circuits and sensors for heterogeneous environments and applications. , 0, , .		12
635	Operational amplifier power optimization for a given total (slewing plus linear) settling time. , 0, , .		8
636	A 110 nA pacemaker sensing channel in CMOS on silicon-on-insulator. , 0, , .		6
637	A physically-based continuous analytical graded-channel SOI nMOSFET model for analog applications. , 0, , .		5
638	Generalization of the integral function method to evaluate distortion in SOI FD MOSFET. , 0, , .		3
639	Capacitive humidity sensor using a polyimide sensing film. , 0, , .		6
640	MOSFET mismatch in weak/moderate inversion: model needs and implications for analog design. , 0, , .		12
641	Measurements, modelling and electrical simulations of lateral PIN photodiodes in thin film-SOI for high quantum efficiency and high selectivity in the UV range. , 0, , .		5
642	DNA electrical detection based on inductor resonance frequency in standard CMOS technology. , 0, , .		0
643	High-sensitivity capacitive humidity sensor using 3-layer patterned polyimide sensing film. , 0, , .		8
644	DNA electrical detection based on inductor resonance frequency in standard CMOS technology. , 0, , .		3
645	Analysis of laterally asymmetric channel design in fully depleted double gate (DG) SOI MOSFETs for high performance analog applications. , 0, , .		1
646	Design of operational transconductance amplifiers with improved gain by using graded-channel SOI nMOSFETs. , 0, , .		0
647	Direct MOSFET parameters extraction using fourier-space techniques. , 0, , .		0
648	Fully CMOS-SOI compatible low-power directional flow sensor. , 0, , .		5

#	ARTICLE	IF	CITATIONS
649	Unusual floating body effect in fully depleted MOSFETs. , 0, , .		6
650	Physical modelling and design of thin film SOI lateral PIN photodiodes for blue DVD-applications. , 0, , .		3
651	Small- and large-signal RF characterization of fully-depleted accumulation-mode varactors for low-voltage LC-VCO SOI design. , 0, , .		2
652	Comparison between nonlinear characteristics of N-channel and P-channel FD SOI MOSFETs. , 0, , .		0
653	On-resistance and harmonic distortion in graded-channel SOI FD MOSFET. , 0, , .		0
654	DNA detection based on capacitive Al/sub 2/O/sub 3//Al microelectrodes. , 0, , .		1
655	Perspective of FinFETs for analog applications. , 0, , .		33
656	Unusual gate current transient behavior in SOI MOSFETs. , 0, , .		2
657	Revised split C-V technique for mobility investigation in advanced devices. , 0, , .		1
658	Specific features of the capacitance and mobility behaviors in finfet structures. , 0, , .		8
659	A low-power 5 GHz CMOS LC-VCO optimized for high-resistivity SOI substrates. , 0, , .		13
660	Ultra-Low Power Flip-Flops for MTCMOS Circuits. , 0, , .		11
661	A Modified EKV PDSOI MOSFETs Model. , 0, , .		0
662	Graded-Channel SOI nMOSFET Model Valid for Harmonic Distortion Evaluation. , 0, , .		2
663	Low-Wavelengths SOI CMOS Photosensors for Biomedical Applications. , 0, , .		1
664	The Effect of Interfacial Charge on the Development of Wafer Bonded Silicon-on-Silicon-Carbide Power Devices. Materials Science Forum, 0, 897, 747-750.	0.3	4