Denis Flandre

List of Publications by Year in descending order

664 papers	9,635 citations	57719 44 h-index	88593 70 g-index
671 all docs	671 docs citations	671 times ranked	5257 citing authors

#	Article	IF	Citations
1	A g/sub m//I/sub D/ based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA. IEEE Journal of Solid-State Circuits, 1996, 31, 1314-1319.	3.5	534
2	Substrate crosstalk reduction using SOI technology. IEEE Transactions on Electron Devices, 1997, 44, 2252-2261.	1.6	251
3	Influence of device engineering on the analog and RF performances of SOI MOSFETs. IEEE Transactions on Electron Devices, 2003, 50, 577-588.	1.6	195
4	Analog/RF performance of multiple gate SOI devices: wideband simulations and characterization. IEEE Transactions on Electron Devices, 2006, 53, 1088-1095.	1.6	156
5	FinFET analogue characterization from DC to 110GHz. Solid-State Electronics, 2005, 49, 1488-1496.	0.8	142
6	Modeling of ultrathin double-gate nMOS/SOI transistors. IEEE Transactions on Electron Devices, 1994, 41, 715-720.	1.6	140
7	Employing Si solar cell technology to increase efficiency of ultraâ€thin Cu(In,Ga)Se₂ solar cells. Progress in Photovoltaics: Research and Applications, 2014, 22, 1023-1029.	4.4	136
8	Interests and Limitations of Technology Scaling for Subthreshold Logic. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 1508-1519.	2.1	132
9	SleepWalker: A 25-MHz 0.4-V Sub-$hbox{mm}^{2}$ 7-$muhbox{W/MHz}$ Microcontroller in 65-nm LP/GP CMOS for Low-Carbon Wireless Sensor Nodes. IEEE Journal of Solid-State Circuits, 2013, 48, 20-32.	3.5	112
10	ULPFA: A New Efficient Design of a Power-Aware Full Adder. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2066-2074.	3.5	103
11	Comparison of TiSi2â€‰,â€‰CoSi2, and NiSi for Thinâ€Film Siliconâ€onâ€Insulator Applications. Journal of the Electrochemical Society, 1997, 144, 2437-2442.	1.3	102
12	A Formal Study of Power Variability Issues and Side-Channel Attacks for Nanoscale Devices. Lecture Notes in Computer Science, 2011, , 109-128.	1.0	101
13	Design of SOI CMOS operational amplifiers for applications up to 300Â°C. IEEE Journal of Solid-State Circuits, 1996, 31, 179-186.	3.5	98
14	Laterally asymmetric channel engineering in fully depleted double gate SOI MOSFETs for high performance analog applications. Solid-State Electronics, 2004, 48, 947-959.	0.8	95
15	A Capacitorless 1T-DRAM on SOI Based on Dynamic Coupling and Double-Gate Operation. IEEE Electron Device Letters, 2008, 29, 795-798.	2.2	87
16	Measurement of threshold voltages of thin-film accumulation-mode PMOS/SOI transistors. IEEE Electron Device Letters, 1991, 12, 682-684.	2.2	84
17	Fully depleted SOI CMOS technology for heterogeneous micropower, high-temperature or RF microsystems. Solid-State Electronics, 2001, 45, 541-549.	0.8	81
18	Improved synthesis of gain-boosted regulated-cascode CMOS stages using symbolic analysis and gm/ID methodology. IEEE Journal of Solid-State Circuits, 1997, 32, 1006-1012.	3.5	76

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19	Sensitive DNA electrical detection based on interdigitated Al/Al2O3 microelectrodes. Sensors and Actuators B: Chemical, 2004, 98, 269-274.	4.0	76
20	Thin films stress extraction using micromachined structures and wafer curvature measurements. Microelectronic Engineering, 2004, 76, 219-226.	1.1	73
21	$g_{m}/I_{m d}$ Method for Threshold Voltage Extraction Applicable in Advanced MOSFETs With Nonlinear Behavior Above Threshold. IEEE Electron Device Letters, 2010, 31, 930-932.	2.2	71
22	Investigating the electronic properties of Al2O3/Cu(In,Ga)Se2 interface. AIP Advances, 2015, 5, .	0.6	69
23	Analog performance and application of graded-channel fully depleted SOI MOSFETs. Solid-State Electronics, 2000, 44, 1219-1222.	0.8	67
24	Electrical detection of DNA hybridization: Three extraction techniques based on interdigitated Al/Al2O3 capacitors. Biosensors and Bioelectronics, 2007, 22, 2199-2207.	5.3	66
25	Modelling and application of fully depleted SOI MOSFETs for low voltage, low power analogue CMOS circuits. Solid-State Electronics, 1996, 39, 455-460.	0.8	62
26	Physical Modeling and Design of Thin-Film SOI Lateral PIN Photodiodes. IEEE Transactions on Electron Devices, 2005, 52, 1116-1122.	1.6	61
27	A 16 x 16 CMOS Capacitive Biosensor Array Towards Detection of Single Bacterial Cell. IEEE Transactions on Biomedical Circuits and Systems, 2016, 10, 364-374.	2.7	61
28	Integral function method for determination of nonlinear harmonic distortion. Solid-State Electronics, 2004, 48, 2225-2234.	0.8	59
29	SOI CMOS Compatible Low-Power Microheater Optimization for the Fabrication of Smart Gas Sensors. IEEE Sensors Journal, 2004, 4, 670-680.	2.4	58
30	Graded-channel fully depleted Silicon-On-Insulator nMOSFET for reducing the parasitic bipolar effects. Solid-State Electronics, 2000, 44, 917-922.	0.8	56
31	A 3-D Analytical Physically Based Model for the Subthreshold Swing in Undoped Trigate FinFETs. IEEE Transactions on Electron Devices, 2007, 54, 2487-2496.	1.6	56
32	Title is missing!. Analog Integrated Circuits and Signal Processing, 1999, 21, 213-228.	0.9	54
33	LDMOS in SOI technology with very-thin silicon film. Solid-State Electronics, 2004, 48, 2263-2270.	0.8	54
34	Compact model for highly-doped double-gate SOI MOSFETs targeting baseband analog applications. Solid-State Electronics, 2007, 51, 655-661.	0.8	54
35	Passivation effects of atomic-layer-deposited aluminum oxide. EPJ Photovoltaics, 2013, 4, 45107.	0.8	54
36	A physically-based C/sub â^ž/-continuous fully-depleted SOI MOSFET model for analog applications. IEEE Transactions on Electron Devices, 1996, 43, 568-575.	1.6	53

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37	New method for determination of harmonic distortion in SOI FD transistors. Solid-State Electronics, 2002, 46, 103-108.	0.8	51
38	Highly reflective rear surface passivation design for ultra-thin Cu(In,Ga)Se 2 solar cells. Thin Solid Films, 2015, 582, 300-303.	0.8	51
39	Subthreshold slope of long-channel, accumulation-mode p-channel SOI MOSFETs. Solid-State Electronics, 1994, 37, 289-294.	0.8	50
40	A new memory effect (MSD) in fully depleted SOI MOSFETs. Solid-State Electronics, 2005, 49, 1547-1555.	0.8	50
41	Ultra-thin body and thin-BOX SOI CMOS technology analog figures of merit. Solid-State Electronics, 2012, 70, 50-58.	0.8	50
42	On the MOSFET Threshold Voltage Extraction by Transconductance and Transconductance-to-Current Ratio Change Methods: Part Iâ€"Effect of Drain Voltage. IEEE Transactions on Electron Devices, 2011, 58, 4180-4188.	1.6	49
43	On the MOSFET Threshold Voltage Extraction by Transconductance and Transconductance-to-Current Ratio Change Methods: Part Iâ€"Effect of Gate-Voltage-Dependent Mobility. IEEE Transactions on Electron Devices, 2011, 58, 4172-4179.	1.6	48
44	Demonstration of the potential of accumulation-mode MOS transistors on SOI substrates for high-temperature operation (150-300 degrees C). IEEE Electron Device Letters, 1993, 14, 10-12.	2.2	47
45	Composite ULP diode fabrication, modelling and applications in multi-Vth FD SOI CMOS technology. Solid-State Electronics, 2004, 48, 1017-1025.	0.8	47
46	Impact of self-heating and substrate effects on small-signal output conductance in UTBB SOI MOSFETs. Solid-State Electronics, 2012, 71, 93-100.	0.8	46
47	Floating effective back-gate effect on the small-signal output conductance of SOI MOSFETs. IEEE Electron Device Letters, 2003, 24, 414-416.	2.2	45
48	Assessment of 28 nm UTBB FD-SOI technology platform for RF applications: Figures of merit and effect of parasitic elements. Solid-State Electronics, 2016, 117, 130-137.	0.8	45
49	Addressing the impact of rear surface passivation mechanisms on ultra-thin Cu(In,Ga)Se2 solar cell performances using SCAPS 1-D model. Solar Energy, 2017, 157, 603-613.	2.9	45
50	Effective mobility in FinFET structures with HfO2 and SiON gate dielectrics and TaN gate electrode. Microelectronic Engineering, 2005, 80, 386-389.	1.1	44
51	UTBB SOI MOSFETs analog figures of merit: Effects of ground plane and asymmetric double-gate regime. Solid-State Electronics, 2013, 90, 56-64.	0.8	44
52	Defect Selfâ€Compensation for Highâ€Mobility Bilayer InGaZnO/In₂O₃ Thinâ€Film Transistor. Advanced Electronic Materials, 2019, 5, 1900125.	2.6	43
53	Substrate impact on threshold voltage and subthreshold slope of sub-32 nm ultra thin SOI MOSFETs with thin buried oxide and undoped channel. Solid-State Electronics, 2010, 54, 213-219.	0.8	42
54	Analysis, Modeling, and Design of a 2.45-GHz RF Energy Harvester for SWIPT IoT Smart Sensors. IEEE Journal of Solid-State Circuits, 2019, 54, 2717-2729.	3.5	41

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55	Innovating SOI memory devices based on floating-body effects. Solid-State Electronics, 2007, 51, 1252-1262.	0.8	40
56	Direct protein detection with a nano-interdigitated array gate MOSFET. Biosensors and Bioelectronics, 2009, 24, 3531-3537.	5.3	40
57	A new interdigitated array microelectrode-oxide-silicon sensor with label-free, high sensitivity and specificity for fast bacteria detection. Sensors and Actuators B: Chemical, 2011, 156, 578-587.	4.0	40
58	Silicon-on-insulator technology for high temperature metal oxide semiconductor devices and circuits. Materials Science and Engineering B: Solid-State Materials for Advanced Technology, 1995, 29, 7-12.	1.7	39
59	Comparison of SOI versus bulk performances of CMOS micropower single-stage OTAs. Electronics Letters, 1994, 30, 1933-1934.	0.5	38
60	Signal-to-noise ratio optimization for detecting bacteria with interdigitated microelectrodes. Sensors and Actuators B: Chemical, 2013, 189, 43-51.	4.0	38
61	Optimisation of rear reflectance in ultra-thin CIGS solar cells towards >20% efficiency. Solar Energy, 2017, 146, 443-452.	2.9	38
62	Carrier Mobility in Undoped Triple-Gate FinFET Structures and Limitations of Its Description in Terms of Top and Sidewall Channel Mobilities. IEEE Transactions on Electron Devices, 2008, 55, 3532-3541.	1.6	37
63	Green SoCs for a sustainable Internet-of-Things. , 2013, , .		37
64	Power-delay product minimization in high-performance 64-bit carry-select adders. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2004, 12, 235-244.	2.1	36
65	Fully Integrated High-Q Switched Capacitor Bandpass Filter with Center Frequency and Bandwidth Tuning. Radio Frequency Integrated Circuits (RFIC) Symposium, IEEE, 2007, , .	0.0	36
66	Technology flavor selection and adaptive techniques for timing-constrained 45nm subthreshold circuits. , 2009, , .		36
67	Extended MASTAR Modeling of DIBL in UTB and UTBB SOI MOSFETs. IEEE Transactions on Electron Devices, 2012, 59, 247-251.	1.6	36
68	Effect of parasitic elements on UTBB FD SOI MOSFETs RF figures of merit. Solid-State Electronics, 2014, 97, 38-44.	0.8	36
69	Surface Passivation of CIGS Solar Cells Using Gallium Oxide. Physica Status Solidi (A) Applications and Materials Science, 2018, 215, 1700826.	0.8	36
70	Immobilization of DNA on CMOS compatible materials. Sensors and Actuators B: Chemical, 2003, 92, 90-97.	4.0	35
71	Planar double-gate SOI MOS devices: Fabrication by wafer bonding over pre-patterned cavities and electrical characterization. Solid-State Electronics, 2007, 51, 231-238.	0.8	34
72	Experimental study of transconductance and mobility behaviors in ultra-thin SOI MOSFETs with standard and thin buried oxides. Solid-State Electronics, 2010, 54, 164-170.	0.8	34

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73	Analog circuit design using graded-channel silicon-on-insulator nMOSFETs. Solid-State Electronics, 2002, 46, 1215-1225.	0.8	33
74	Perspective of FinFETs for analog applications. , 0, , .		33
75	Miniaturized Wireless Sensing System for Real-Time Breath Activity Recording. IEEE Sensors Journal, 2010, 10, 178-184.	2.4	33
76	An Asymmetric Channel SOI nMOSFET for Reducing Parasitic Effects and Improving Output Characteristics. Electrochemical and Solid-State Letters, 1999, 3, 50.	2.2	32
77	Advantages of the Graded-Channel SOI FD MOSFET for Application as a Quasi-Linear Resistor. IEEE Transactions on Electron Devices, 2005, 52, 967-972.	1.6	32
78	Electrical characterization of true Silicon-On-Nothing MOSFETs fabricated by Si layer transfer over a pre-etched cavity. Solid-State Electronics, 2007, 51, 1238-1244.	0.8	32
79	A Capacitance-to-Frequency Converter With On-Chip Passivated Microelectrodes for Bacteria Detection in Saline Buffers Up to 575 MHz. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 159-163.	2.2	32
80	Capacitive biosensing of bacterial cells: Analytical model and numerical simulations. Sensors and Actuators B: Chemical, 2015, 211, 428-438.	4.0	32
81	Moderate inversion model of ultrathin double-gate nMOS/SOI transistors. Solid-State Electronics, 1995, 38, 171-176.	0.8	31
82	A new analytical model for the two-terminal MOS capacitor on SOI substrate. IEEE Electron Device Letters, 1988, 9, 296-299.	2.2	30
83	Nanometer MOSFET effects on the minimum-energy point of 45nm subthreshold logic. , 2009, , .		30
84	Can we connect trillions of IoT sensors in a sustainable way? A technology/circuit perspective (Invited). , 2015, , .		30
85	Lytic enzymes as selectivity means for label-free, microfluidic and impedimetric detection of whole-cell bacteria using ALD-Al2O3 passivated microelectrodes. Biosensors and Bioelectronics, 2015, 67, 154-161.	5.3	30
86	Extended theoretical analysis of the steady-state linear behaviour of accumulation-mode, long-channel p-MOSFETs on SOI substrates. Solid-State Electronics, 1992, 35, 1085-1092.	0.8	29
87	Low Leakage SOI CMOS Static Memory Cell With Ultra-Low Power Diode. IEEE Journal of Solid-State Circuits, 2007, 42, 689-702.	3.5	29
88	Harvesting the potential of nano-CMOS for lightweight cryptography: an ultra-low-voltage 65Ânm AES coprocessor for passive RFID tags. Journal of Cryptographic Engineering, 2011, 1, 79-86.	1.5	29
89	Wide frequency band assessment of 28nm FDSOI technology platform for analogue and RF applications. Solid-State Electronics, 2015, 108, 47-52.	0.8	29
90	Extended study of crosstalk in SOI-SIMOX substrates. , 0, , .		28

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91	SOI n-MOSFET low-frequency noise measurements and modeling from room temperature up to 250Â°C. IEEE Transactions on Electron Devices, 2002, 49, 1289-1295.	1.6	28
92	Understanding hydrogen and nitrogen doping on active defects in amorphous In-Ga-Zn-O thin film transistors. Applied Physics Letters, 2018, 112, .	1.5	28
93	Detection mechanism in highly sensitive ZnO nanowires network gas sensors. Sensors and Actuators B: Chemical, 2019, 297, 126602.	4.0	28
94	On the high-temperature subthreshold slope of thin-film SOI MOSFETs. IEEE Electron Device Letters, 2002, 23, 148-150.	2.2	27
95	A 65 nm 0.5 V DPS CMOS Image Sensor With 17 pJ/Frame.Pixel and 42 dB Dynamic Range for Ultra-Low-Power SoCs. IEEE Journal of Solid-State Circuits, 2015, 50, 2419-2430.	3.5	27
96	28-nm FD-SOI CMOS RF Figures of Merit Down to 4.2 K. IEEE Journal of the Electron Devices Society, 2020, 8, 646-654.	1.2	27
97	Characterization of quantum efficiency, effective lifetime and mobility in thin film ungated SOI lateral PIN photodiodes. Solid-State Electronics, 2007, 51, 337-342.	0.8	26
98	Specific features of multiple-gate MOSFET threshold voltage and subthreshold slope behavior at high temperatures. Solid-State Electronics, 2007, 51, 1185-1193.	0.8	26
99	Harmonic distortion analysis of double gate graded-channel MOSFETs operating in saturation. Microelectronics Journal, 2008, 39, 1663-1670.	1.1	26
100	Characterization of high-efficiency multi-crystalline silicon in industrial production. Solar Energy Materials and Solar Cells, 2013, 117, 225-230.	3.0	26
101	A Sizing Methodology for On-Chip Switched-Capacitor DC/DC Converters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 1597-1606.	3.5	26
102	Low Power Analog CMOS for Cardiac Pacemakers. , 2004, , .		25
103	Analysis of quasi double gate method for performance prediction of deep submicron double gate SOI MOSFETs. Semiconductor Science and Technology, 2005, 20, 423-429.	1.0	25
104	Information Theoretic and Security Analysis of a 65-Nanometer DDSLL AES S-Box. Lecture Notes in Computer Science, 2011, , 223-239.	1.0	25
105	Evidence of different conduction mechanisms in accumulation-mode p-channel SOI MOSFET's at room and liquid-helium temperatures. IEEE Transactions on Electron Devices, 1993, 40, 727-732.	1.6	24
106	Frequency Variation of the Small-Signal Output Conductance of Decananometer MOSFETs Due to Substrate Crosstalk. IEEE Electron Device Letters, 2007, 28, 419-421.	2.2	24
107	Analysis and minimization of practical energy in 45nm subthreshold logic circuits. , 2008, , .		24
108	Optimization of Back Contact Grid Size in Al₂O₃-Rear-Passivated Ultrathin CIGS PV Cells by 2-D Simulations. IEEE Journal of Photovoltaics, 2020, 10, 1908-1917.	1.5	24

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109	SOI CMOS TRANSISTORS FOR RF AND MICROWAVE APPLICATIONS. International Journal of High Speed Electronics and Systems, 2001, 11, 1159-1248.	0.3	23
110	Determination of film and surface recombination in thin-film SOI devices using gated-diode technique. Solid-State Electronics, 2004, 48, 389-399.	0.8	23
111	A Simple Method for Measuring Si-Fin Sidewall Roughness by AFM. IEEE Nanotechnology Magazine, 2009, 8, 611-616.	1.1	23
112	Physics of Gate Modulated Resonant Tunneling (RT)-FETs: Multi-barrier MOSFET for steep slope and high on-current. Solid-State Electronics, 2011, 59, 50-61.	0.8	23
113	Compact diamond MOSFET model accounting for PAMDLE applicable down 150Ânm node. Electronics Letters, 2014, 50, 1618-1620.	0.5	23
114	Charge-sheet modelling of MOS I-V fundamental nonlinearities in MOSFET-C continuous-time filters. Electronics Letters, 1995, 31, 1419-1420.	0.5	22
115	Accurate effective mobility extraction by split C-V technique in SOI MOSFETs: suppression of the influence of floating-body effects. IEEE Electron Device Letters, 2005, 26, 749-751.	2.2	22
116	Thin film fully-depleted SOI four-gate transistors. Solid-State Electronics, 2007, 51, 278-284.	0.8	22
117	Silicon-on-Nothing MOSFETs: An efficient solution for parasitic substrate coupling suppression in SOI devices. Applied Surface Science, 2008, 254, 6168-6173.	3.1	22
118	Dynamic body potential variation in FD SOI MOSFETs operated in deep non-equilibrium regime: Model and applications. Solid-State Electronics, 2010, 54, 104-114.	0.8	22
119	Energy-Band Engineering for Improved Charge Retention in Fully Self-Aligned Double Floating-Gate Single-Electron Memories. Nano Letters, 2011, 11, 4520-4526.	4.5	22
120	Automated Design of a 13.56 MHz 19 ÂµW Passive Rectifier With 72% Efficiency Under 10 ÂµA load. IEEE Journal of Solid-State Circuits, 2016, 51, 1290-1301.	3.5	22
121	Analysis of floating substrate effects on the intrinsic gate capacitance of SOI MOSFETSs using two-dimensional device simulation. IEEE Transactions on Electron Devices, 1993, 40, 1789-1796.	1.6	21
122	Self-cascode SOI versus graded-channel SOI MOS transistors. IET Circuits, Devices and Systems, 2006, 153, 461.	0.6	21
123	Compact model for single event transients and total dose effects at high temperatures for partially depleted SOI MOSFETs. Microelectronics Reliability, 2010, 50, 1852-1856.	0.9	21
124	Asymmetric self-cascode configuration to improve the analog performance of SOI nMOS transistors. , 2011, , .		21
125	A 25MHz 7μW/MHz ultra-low-voltage microcontroller SoC in 65nm LP/GP CMOS for low-carbon wireless sensor nodes. , 2012, , .		21
126	Out-of-plane MEMS-based mechanical airflow sensor co-integrated in SOI CMOS technology. Sensors and Actuators A: Physical, 2014, 206, 67-74.	2.0	21

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127	Diamond layout style impact on SOI MOSFET in high temperature environment. Microelectronics Reliability, 2015, 55, 783-788.	0.9	21
128	Comparison of self-heating and its effect on analogue performance in 28 nm bulk and FDSOI. Solid-State Electronics, 2016, 115, 219-224.	0.8	21
129	Light management design in ultra-thin chalcopyrite photovoltaic devices by employing optical modelling. Solar Energy Materials and Solar Cells, 2019, 200, 109933.	3.0	21
130	28â€¯nm FDSOI analog and RF Figures of Merit at N2 cryogenic temperatures. Solid-State Electronics, 2019, 159, 77-82.	0.8	21
131	Gate-all-around OTA's for rad-hard and high-temperature analog applications. IEEE Transactions on Nuclear Science, 1999, 46, 1242-1249.	1.2	20
132	Investigation of Deep Submicron Single and Double Gate SOI MOSFETs in Accumulation Mode for Enhanced Performance. Electrochemical and Solid-State Letters, 2001, 4, G28.	2.2	20
133	0.25 Î¼m fully depleted SOI MOSFETs for RF mixed analog-digital circuits, including a comparison with partially depleted devices with relation to high frequency noise parameters. Solid-State Electronics, 2002, 46, 379-386.	0.8	20
134	Low-swing current mode logic (LSCML): A new logic style for secure and robust smart cards against power analysis attacks. Microelectronics Journal, 2006, 37, 997-1006.	1.1	20
135	Substrate Bias Effect Linked to Parasitic Series Resistance in Multiple-Gate SOI MOSFETs. IEEE Electron Device Letters, 2007, 28, 834-836.	2.2	20
136	Using diamond layout style to boost MOSFET frequency response of analogue IC. Electronics Letters, 2014, 50, 398-400.	0.5	20
137	Fully depleted SOI-CMOS technology for high temperature IC applications. Materials Science and Engineering B: Solid-State Materials for Advanced Technology, 1997, 46, 1-7.	1.7	19
138	Potential and modeling of 1-Î¼m SOI CMOS operational transconductance amplifiers for applications up to 1 GHz. IEEE Journal of Solid-State Circuits, 1998, 33, 640-643.	3.5	19
139	New experiments on the electrodeposition of iron in porous silicon. Microelectronics Reliability, 2000, 40, 877-879.	0.9	19
140	Integrated sensor and electronic circuits in fully depleted SOI technology for high-temperature applications. IEEE Transactions on Industrial Electronics, 2001, 48, 272-280.	5.2	19
141	A method to extract mobility degradation and total series resistance of fully-depleted SOI MOSFETs. IEEE Transactions on Electron Devices, 2002, 49, 82-88.	1.6	19
142	Floating-Body SOI Memory: Concepts, Physics and Challenges. ECS Transactions, 2009, 19, 243-256.	0.3	19
143	Characteristics of nMOS/GAA (Gate-All-Around) transistors near threshold. Microelectronic Engineering, 1992, 19, 815-818.	1.1	18
144	Radiation-hard design for SOI MOS inverters. IEEE Transactions on Nuclear Science, 1994, 41, 402-407.	1.2	18

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145	Building Ultra-Low-Power Low-Frequency Digital Circuits with High-Speed Devices. , 2007, , .		18
146	A Self-Tuning Inductive Powering System for Biomedical Implants. Procedia Engineering, 2011, 25, 1585-1588.	1.2	18
147	Fully-Automated and Portable Design Methodology for Optimal Sizing of Energy-Efficient CMOS Voltage Rectifiers. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2011, 1, 141-149.	2.7	18
148	Illuminated to dark ratio improvement in lateral SOI PIN photodiodes at high temperatures. Semiconductor Science and Technology, 2014, 29, 075008.	1.0	18
149	On the improvement of DC analog characteristics of FD SOI transistors by using asymmetric self-cascode configuration. Solid-State Electronics, 2016, 117, 152-160.	0.8	18
150	SleepRunner: A 28-nm FDSOI ULP Cortex-M0 MCU With ULL SRAM and UFBR PVT Compensation for 2.6â€“3.6-Î¼W/DMIPS 40â€“80-MHz Active Mode and 131-nW/kB Fully Retentive Deep-Sleep Mode. IEEE Journal of Solid-State Circuits, 2021, 56, 2256-2269.	3.5	18
151	Design of thin-film fully-depleted SOI CMOS analog circuits significantly outperforming bulk implementations. , 0, , .		17
152	Reduction of gate-to-channel tunneling current in FinFET structures. Solid-State Electronics, 2007, 51, 1466-1472.	0.8	17
153	On the gm/ID-based approaches for threshold voltage extraction in advanced MOSFETs and their application to ultra-thin body SOI MOSFETs. Solid-State Electronics, 2014, 97, 52-58.	0.8	17
154	A modified g m /I D design methodology for deeply scaled CMOS technologies. Analog Integrated Circuits and Signal Processing, 2014, 78, 771-784.	0.9	17
155	Resonant dielectrophoresis and electrohydrodynamics for high-sensitivity impedance detection of whole-cell bacteria. Lab on A Chip, 2015, 15, 3183-3191.	3.1	17
156	Junctionless nanowire transistors operation at temperatures down to 4.2 K. Semiconductor Science and Technology, 2016, 31, 114001.	1.0	17
157	A battery-less BLE smart sensor for room occupancy tracking supplied by 2.45-GHz wireless power transfer. The Integration VLSI Journal, 2019, 67, 8-18.	1.3	17
158	Special Features of the Back-Gate Effects in Ultra-Thin Body SOI MOSFETs. Engineering Materials, 2011, , 323-339.	0.3	17
159	A physically-based C/sub â^ž/-continuous model for accumulation-mode SOI pMOSFETs. IEEE Transactions on Electron Devices, 1999, 46, 2295-2303.	1.6	16
160	Bulk and surface micromachined MEMS in thin film SOI technology. Electrochimica Acta, 2007, 52, 2850-2861.	2.6	16
161	High-efficiency solar cell embedded in SOI substrate for ULP autonomous circuits. , 2009, , .		16
162	Method for fabricating third generation photovoltaic cells based on Si quantum dots using ion implantation into SiO2. Journal of Applied Physics, 2011, 109, .	1.1	16

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163	Wide frequency band assessment of 28 nm FDSOI technology platform for analogue and RF applications. , 2014, , .		16
164	Gradient importance sampling: An efficient statistical extraction methodology of high-sigma SRAM dynamic characteristics. , 2018, , .		16
165	Impact of hydrogen dopant incorporation on InGaZnO, ZnO and In₂O₃ thin film transistors. Physical Chemistry Chemical Physics, 2020, 22, 1591-1597.	1.3	16
166	Measurement of intrinsic gate capacitances of SOI MOSFET's. IEEE Electron Device Letters, 1990, 11, 291-293.	2.2	15
167	Comparison of DNA detection methods using nanoparticles and silver enhancement. IET Nanobiotechnology, 2005, 152, 3.	2.1	15
168	Characterization of ultrathin SOI film and application to short channel MOSFETs. Nanotechnology, 2008, 19, 165703.	1.3	15
169	Scaling trends of the AES S-box low power consumption in 130 and 65 nm CMOS technology nodes. , 2009, , .		15
170	Implementation of the symmetric doped doubleâ€gate MOSFET model in Verilogâ€A for circuit simulation. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2010, 23, 88-106.	1.2	15
171	The detrimental impact of negative Celsius temperature on ultra-low-voltage CMOS logic. , 2010, , .		15
172	Contribution of carrier tunneling and gate induced drain leakage effects to the gate and drain currents of finâ€“shaped fieldâ€“effect transistors. Journal of Applied Physics, 2011, 109, .	1.1	15
173	Room temperature atomic layer deposition of Al2O3 and replication of butterfly wings for photovoltaic application. Journal of Vacuum Science and Technology A: Vacuum, Surfaces and Films, 2012, 30, .	0.9	15
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