Hamed Aminzadeh

List of Publications by Year
in descending order

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42	336	840776 11	996975 15
papers	citations	h-index	g-index

42	42	42	123
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Threeâ€stage nestedâ€Millerâ€compensated operational amplifiers: Analysis, design, and optimization based on settling time. International Journal of Circuit Theory and Applications, 2011, 39, 573-587.	2.0	20
2	Design of high-speed two-stage cascode-compensated operational amplifiers based on settling time and open-loop parameters. The Integration VLSI Journal, 2008, 41, 183-192.	2.1	18
3	Hybrid cascode feedforward compensation for nano-scale low-power ultra-area-efficient three-stage amplifiers. Microelectronics Journal, 2013, 44, 1201-1207.	2.0	17
4	MOSFET-only pipelined analogue-to-digital converters: non-linearity compensation by digital calibration. International Journal of Electronics, 2014, 101, 158-173.	1.4	17
5	Dual loop cascodeâ€Miller compensation with damping factor control unit for threeâ€stage amplifiers driving ultralarge load capacitors. International Journal of Circuit Theory and Applications, 2019, 47, 1-18.	2.0	17
6	Selfâ€biased nanoâ€power fourâ€transistor current and voltage reference with a single resistor. Electronics Letters, 2020, 56, 282-284.	1.0	17
7	Systematic circuit design and analysis using generalised g _m / I _D functions of MOS devices. IET Circuits, Devices and Systems, 2020, 14, 432-443.	1.4	15
8	Hybrid cascode compensation with current amplifiers for nano-scale three-stage amplifiers driving heavy capacitive loads. Analog Integrated Circuits and Signal Processing, 2015, 83, 331-341.	1.4	14
9	Allâ€“MOS self-powered subthreshold voltage reference with enhanced line regulation. AEU - International Journal of Electronics and Communications, 2020, 122, 153245.	2.9	13
10	0.7-V supply, 21-nW Allâ€“MOS voltage reference using a MOS-Only current-driven reference core in digital CMOS. Microelectronics Journal, 2020, 102, 104841.	2.0	12
11	Design of Two-Stage Miller-Compensated Amplifiers Based on an Optimized Settling Model. , 2007, , .		11
12	ON THE POWER EFFICIENCY OF CASCODE COMPENSATION OVER MILLER COMPENSATION IN TWO-STAGE OPERATIONAL AMPLIFIERS. Journal of Circuits, Systems and Computers, 2008, 17, 1-13.	1.5	11
13	Design of low-power single-stage operational amplifiers based on an optimized settling model. Analog Integrated Circuits and Signal Processing, 2009, 58, 153-160.	1.4	11
14	Low-Dropout Voltage Source: An Alternative Approach for Low-Dropout Voltage Regulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 413-417.	3.0	11
15	Miller Compensation: Optimal Design for Operational Amplifiers with a Required Settling Time. Circuits, Systems, and Signal Processing, 2014, 33, 2675-2694.	2.0	11
16	Study of capacitance nonlinearity in nano-scale multi-stage MOSFET-only sigma-delta modulators. AEU - International Journal of Electronics and Communications, 2018, 85, 150-158.	2.9	10
17	Evaluation of the pole expressions of nano-scale multistage amplifiers based on equivalent output impedance. AEU - International Journal of Electronics and Communications, 2017, 72, 243-251.	2.9	9
18	A Methodology to Derive a Symbolic Transfer Function for Multistage Amplifiers. IEEE Access, 2022, 10, 14062-14075.	4.2	9

#	Article	IF	Citations
19	On the Linearization of MOSFET Capacitors. , 2007, , .		8
20	A low-voltage high-speed high-linearity MOSFET-only analog bootstrapped switch for sample-and-hold circuits. , 2015, , .		7
21	A Low-Cost Tiny-Size Successive Approximation ADC for Applications Requiring Low-Resolution Conversion with Moderate Sampling Rate. Circuits, Systems, and Signal Processing, 2019, 38, 242-258.	2.0	7
22	Frequency Compensation of Three-Stage OTAs to Achieve Very Wide Capacitive Load Range. IEEE Access, 2022, 10, 70675-70687.	4.2	7
23	MOSFET-ONLY TWO-STAGE OPERATIONAL AMPLIFIERS WITH MILLER COMPENSATION: DESIGN AND FABRICATION IN NANO-SCALE CMOS. Journal of Circuits, Systems and Computers, 2013, 22, 1350065.	1.5	6
24	A nano-power sub-bandgap voltage and current reference topology with no amplifier. AEU - International Journal of Electronics and Communications, 2022, 148, 154174.	2.9	6
25	Design of High-Resolution MOSFET-Only Pipelined ADCs with Digital Calibration. , 2007, , .		5
26	Low-cost area-efficient low-dropout regulators using MOSFET capacitors. IEICE Electronics Express, 2008, 5, 610-616.	0.8	5
27	Low-dropout regulators: Hybrid-cascode compensation to improve stability in nano-scale CMOS technologies. , 2011, , .		5
28	Digital extraction of quantization error and its applications to successful design of sigma-delta modulator. Analog Integrated Circuits and Signal Processing, 2018, 94, 413-425.	1.4	5
29	Analysis of multistage amplifiers with hybrid cascode feedforward compensation using a modified model for load impedance. Analog Integrated Circuits and Signal Processing, 2018, 95, 271-282.	1.4	5
30	Global impedance attenuation network for multistage OTAs driving a broad range of load capacitor. International Journal of Circuit Theory and Applications, 2020, 48, 181-197.	2.0	5
31	Subthreshold reference circuit with curvature compensation based on the channel length modulation of MOS devices. International Journal of Circuit Theory and Applications, 2022, 50, 1082-1100.	2.0	5
32	Nano-scale area-efficient G_mâ€“C filters using MOS capacitors. International Journal of Electronics Letters, 2019, 7, 311-320.	1.2	4
33	Area-efficient low-cost low-dropout regulators using MOS capacitors. , 2008, , .		3
34	Optimal placement of phasor measurement units to obtain network observability using a hybrid PSOâ€“GSA algorithm. Australian Journal of Electrical and Electronics Engineering, 2015, 12, 342-349.	1.2	3
35	Nano-Scale Silicon Quantum Dot-Based Single-Electron Transistors and Their Application to Design of Analog-to-Digital Convertors at Room Temperature. Journal of Circuits, Systems and Computers, 2017, 26, 1750201.	1.5	3
36	Design of two-stage MOSFET-only operational amplifiers. , 2008, , .		2

#	Article	IF	Citations
37	Low-dropout voltage reference: An approach to buffered architectures with low sensitivity. , 2010, , .		1
38	Hybrid cascode compensation with feedforward stage for high-speed area-efficient three-stage CMOS amplifiers. Analog Integrated Circuits and Signal Processing, 2014, 78, 253-256.	1.4	1
39	A reliable model for the compensation loop of multistage amplifiers at high frequency. Circuit World, 2019, 45, 268-278.	0.9	0
40	Hybrid cascode compensation with Q-factor control module for three-stage OTAs driving ultra-large load capacitors. Circuit World, 2021, 47, 345-356.	0.9	0
41	Circuit-level Design of a Power Supply Unit with Extra Low-noise Output for Portable Integrated SoCs. International Journal of Computer Applications, 2012, 50, 1-6.	0.2	0
42	3.48-nW 58.4ppm/^{â˜}C Sub-threshold CVR with Four Transistors and Two Resistors. Journal of Circuits, Systems and Computers, 0, , .	1.5	0