Jaume Abella

List of Publications by Year
in descending order

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Version: 2024-02-01

202 papers	2,307 citations	687363 13 h-index	610901 24 g-index
205 all docs	205 docs citations	205 times ranked	833 citing authors

#	Article	IF	Citations
1	SafeDE: A Low-Cost Hardware Solution to Enforce Diverse Redundancy in Multicores. IEEE Transactions on Device and Materials Reliability, 2022, 22, 111-119.	2.0	1
2	On the Safe Deployment of Matrix Multiplication in Massively Parallel Safety-Related Systems. Applied Sciences (Switzerland), 2022, 12, 3779.	2.5	2
3	De-RISC: A Complete RISC-V Based Space-Grade Platform. , 2022, , .		5
4	SafeDM: a Hardware Diversity Monitor for Redundant Execution on Non-Lockstepped Cores. , 2022, , .		3
5	Worst-Case Energy Consumption: A New Challenge for Battery-Powered Critical Devices. IEEE Transactions on Sustainable Computing, 2021, 6, 522-530.	3.1	1
6	Surrogate Applications for Early Design Stage Multicore Contention Modeling. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 109-116.	4.6	2
7	Achieving diverse redundancy for GPU Kernels. IEEE Transactions on Emerging Topics in Computing, 2021, , 1-1.	4.6	1
8	Empirical Evidence for MPSoCs in Critical Systems: The Case of NXP's T2080 Cache Coherence. , 2021, , .		3
9	MUCH. , 2021, , .		0
10	Security, Reliability and Test Aspects of the RISC-V Ecosystem. , 2021, , .		3
11	SafeSU: an Extended Statistics Unit for Multicore Timing Interference. , 2021, , .		8
12	SafeTI: a Hardware Traffic Injector for MPSoC Functional and Timing Validation. , 2021, , .		4
13	Performance Analysis and Optimization Opportunities for NVIDIA Automotive GPUs. Journal of Parallel and Distributed Computing, 2021, 152, 21-32.	4.1	11
14	SafeDE: a flexible Diversity Enforcement hardware module for light-lockstepping. , 2021, , .		7
15	De-RISC: the First RISC-V Space-Grade Platform for Safety-Critical Systems. , 2021, , .		11
16	Multi-core Devices for Safety-critical Systems. ACM Computing Surveys, 2021, 53, 1-38.	23.0	25
17	Predictive Reliability and Fault Management in Exascale Systems. ACM Computing Surveys, 2021, 53, 1-32.	23.0	11
18	Enabling Unit Testing of Already-Integrated AI Software Systems: The Case of Apollo for Autonomous Driving. , 2021, , .		4

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19	Towards functional safety compliance of matrixâ€“matrix multiplication for machine learning-based autonomous systems. Journal of Systems Architecture, 2021, 121, 102298.	4.3	6
20	PRL: Standardizing Performance Monitoring Library for High-Integrity Real-Time Systems. , 2021, , .		0
21	Probabilistic Worst-Case Timing Analysis. ACM Computing Surveys, 2020, 52, 1-35.	23.0	43
22	The ECSEL FRACTAL Project: A Cognitive Fractal and Secure edge based on a unique Open-Safe-Reliable-Low Power Hardware Platform. , 2020, , .		6
23	Software-Only Triple Diverse Redundancy on GPUs for Autonomous Driving Platforms. , 2020, , .		4
24	Modeling Contention Interference in Crossbar-based Systems via Sequence-Aware Pairing (SeAP). , 2020, , .		1
25	SELENE: Self-Monitored Dependable Platform for High-Performance Safety-Critical Systems. , 2020, , .		14
26	HRM: Merging Hardware Event Monitors for Improved Timing Analysis of Complex MPSoCs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3662-3673.	2.7	2
27	A Cross-Layer Review of Deep Learning Frameworks to Ease Their Optimization and Reuse. , 2020, , .		9
28	On the Use of Probabilistic Worst-Case Execution Time Estimation for Parallel Applications in High Performance Systems. Mathematics, 2020, 8, 314.	2.2	4
29	GPU4S: Embedded GPUs in space - Latest project updates. Microprocessors and Microsystems, 2020, 77, 103143.	2.8	9
30	Timing of Autonomous Driving Software: Problem Analysis and Prospects for Future Solutions. , 2020, , .		28
31	En-Route. , 2020, , .		3
32	IntPred. , 2020, , .		1
33	Workshop on High-performance Computing Platforms for Dependable Autonomous Systems. , 2020, , .		0
34	Software-only based Diverse Redundancy for ASIL-D Automotive Applications on Embedded HPC Platforms. , 2020, , .		13
35	On the reliability of hardware event monitors in MPSoCs for critical domains. , 2020, , .		2
36	CleanET. , 2020, , .		1

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37	An Academic RISC-V Silicon Implementation Based on Open-Source Components. , 2020, , .		7
38	Randomization for Safer, more Reliable and Secure, High-Performance Automotive Processors. IEEE Design and Test, 2019, 36, 39-47.	1.2	0
39	Assessing the Adherence of an Industrial Autonomous Driving Framework to ISO 26262 Software Guidelines. , 2019, , .		15
40	Accurate ILP-Based Contention Modeling on Statically Scheduled Multicore Systems. , 2019, , .		2
41	An Approach for Detecting Power Peaks During Testing and Breaking Systematic Pathological Behavior. , 2019, , .		0
42	AURIX TC277 Multicore Contention Model Integration for Automotive Applications. , 2019, , .		2
43	LAEC: Look-Ahead Error Correction Codes in Embedded Processors L1 Data Cache. , 2019, , .		1
44	Time-Randomized Wormhole NoCs for Critical Applications. ACM Journal on Emerging Technologies in Computing Systems, 2019, 15, 1-23.	2.3	2
45	Towards limiting the impact of timing anomalies in complex real-time processors. , 2019, , .		1
46	Software Timing Analysis for Complex Hardware with Survivability and Risk Analysis. , 2019, , .		1
47	Performance Analysis and Optimization of Automotive GPUs. , 2019, , .		5
48	GPU4S: Embedded GPUs in Space. , 2019, , .		15
49	High-Integrity GPU Designs for Critical Real-Time Automotive Systems. , 2019, , .		15
50	STT-MRAM for real-time embedded systems. , 2019, , .		5
51	Software-only Diverse Redundancy on GPUs for Autonomous Driving Platforms. , 2019, , .		12
52	Maximum-Contention Control Unit (MCCU): Resource Access Count and Contention Time Enforcement. , 2019, , .		10
53	Modeling the Impact of Process Variations in Worst-Case Energy Consumption Estimation. , 2019, , .		2
54	Increasing the Reliability of Software Timing Analysis for Cache-Based Processors. IEEE Transactions on Computers, 2019, 68, 836-851.	3.4	3

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55	Locality-aware cache random replacement policies. Journal of Systems Architecture, 2019, 93, 48-61.	4.3	1
56	Multicore Early Design Stage Guaranteed Performance Estimates for the Space Domain. , 2019, , .		0
57	On assessing the viability of probabilistic scheduling with dependent tasks. , 2019, , .		0
58	High-Integrity Performance Monitoring Units in Automotive Chips for Reliable Timing V&V. IEEE Micro, 2018, 38, 56-65.	1.8	11
59	Design and integration of hierarchical-placement multi-level caches for real-time systems. , 2018, , .		2
60	Reconciling Time Predictability and Performance in Future Computing Systems. IEEE Design and Test, 2018, 35, 48-56.	1.2	3
61	Assessing Time Predictability Features of ARM Big. LITTLE Multicores. , 2018, , .		2
62	RPR. , 2018, , .		2
63	Measurement-based cache representativeness on multipath programs. , 2018, , .		1
64	Safety-Related Challenges and Opportunities for GPUs in the Automotive Domain. IEEE Micro, 2018, 38, 46-55.	1.8	22
65	NoCo: ILP-Based Worst-Case Contention Estimation for Mesh Real-Time Manycores. , 2018, , .		6
66	Modelling Multicore Contention on the AURIXâ„¢ TC27x. , 2018, , .		10
67	Measurement-Based Cache Representativeness on Multipath Programs. , 2018, , .		0
68	A Reliable Statistical Analysis of the Best-Fit Distribution for High Execution Times. , 2018, , .		2
69	Modelling multicore contention on the AURIX TM TC27x. , 2018, , .		5
70	Cache side-channel attacks and time-predictability in high-performance critical real-time systems. , 2018, , .		7
71	EOmesh: Combined Flow Balancing and Deterministic Routing for Reduced WCET Estimates in Embedded Real-Time Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2451-2461.	2.7	2
72	Fitting Software Execution-Time Exceedance into a Residual Random Fault in ISO-26262. IEEE Transactions on Reliability, 2018, 67, 1314-1327.	4.6	7

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73	DReAM. ACM Transactions on Design Automation of Electronic Systems, 2017, 22, 1-26.	2.6	2
74	Aging Assessment and Design Enhancement of Randomized Cache Memories. IEEE Transactions on Device and Materials Reliability, 2017, 17, 32-41.	2.0	3
75	Measurement-Based Worst-Case Execution Time Estimation Using the Coefficient of Variation. ACM Transactions on Design Automation of Electronic Systems, 2017, 22, 1-29.	2.6	47
76	EPC Enacted: Integration in an Industrial Toolbox and Use against a Railway Application. , 2017, , .		0
77	Adapting TDMA arbitration for measurement-based probabilistic timing analysis. Microprocessors and Microsystems, 2017, 52, 188-201.	2.8	1
78	Probabilistic timing analysis on time-randomized platforms for the space domain. , 2017, , .		13
79	Boosting Guaranteed Performance in Wormhole NoCs with Probabilistic Timing Analysis. , 2017, , .		1
80	Modelling bus contention during system early design stages. , 2017, , .		0
81	On uses of extreme value theory fit for industrial-quality WCET analysis. , 2017, , .		6
82	Design and implementation of a fair credit-based bandwidth sharing scheme for buses. , 2017, , .		4
83	Dynamic software randomisation: Lessons learnec from an aerospace case study. , 2017, , .		6
84	On the assessment of probabilistic WCET estimates reliability for arbitrary programs. Eurasip Journal on Embedded Systems, 2017, 2017, .	1.2	4
85	Computing Safe Contention Bounds for Multicore Resources with Round-Robin and FIFO Arbitration. IEEE Transactions on Computers, 2017, 66, 586-600.	3.4	10
86	SEDEA: A Sensible Approach to Account DRAM Energy in Multicore Systems. , 2017, , .		0
87	Work-in-Progress Paper: An Analysis of the Impact of Dependencies on Probabilistic Timing Analysis and Task Scheduling. , 2017, , .		1
88	On the tailoring of CAST-32A certification guidance to real COTS multicore architectures. , 2017, , .		16
89	DIMP. , 2017, , .		7
90	Software Time Reliability in the Presence of Cache Memories. Lecture Notes in Computer Science, 2017, , 233-249.	1.3	2

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91	Random modulo. , 2016, , .		20
92	A confidence assessment of WCET estimates for software time randomized caches. , 2016, , .		3
93	Modelling Probabilistic Cache Representativeness in the Presence of Arbitrary Access Patterns. , 2016, , .		10
94	Contention-aware performance monitoring counter support for real-time MPSoCs. , 2016, , .		10
95	Modeling RTL fault models behavior to increase the confidence on TSIM-based fault injection. , 2016, , .		0
96	Modeling High-Performance Wormhole NoCs for Critical Real-Time Embedded Systems. , 2016, , .		10
97	Data Bus Slicing for Contention-Free Multicore Real-Time Memory Systems. , 2016, , .		0
98	Fitting processor architectures for measurement-based probabilistic timing analysis. Microprocessors and Microsystems, 2016, 47, 287-302.	2.8	29
99	Modelling the confidence of timing analysis for time randomised caches. , 2016, , .		4
100	Resilient random modulo cache memories for probabilistically-analyzable real-time systems. , 2016, , .		3
101	PROXIMA: Improving Measurement-Based Timing Analysis through Randomisation and Probabilistic Analysis. , 2016, , .		20
102	pTNoC: Probabilistically Time-Analyzable Tree-Based NoC for Mixed-Criticality Systems. , 2016, , .		5
103	TASA. , 2016, , .		11
104	Improving Early Design Stage Timing Modeling in Multicore Based Real-Time Systems. , 2016, , .		3
105	Parallelizing Industrial Hard Real-Time Applications for the parMERASA Multicore. Transactions on Embedded Computing Systems, 2016, 15, 1-27.	2.9	14
106	Improving Performance Guarantees in Wormhole Mesh NoC Designs. , 2016, , .		4
107	Sensible Energy Accounting with Abstract Metering for Multicore Systems. Transactions on Architecture and Code Optimization, 2016, 12, 1-26.	2.0	1
108	Enabling TDMA Arbitration in the Context of MBPTA. , 2015, , .		5

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109	EPC: Extended Path Coverage for Measurement-Based Probabilistic Timing Analysis. , 2015, , .		12
110	Low-cost Checkpointing in Automotive Safety-Relevant Systems. , 2015, , .		7
111	Timing Analysis of an Avionics Case Study on Complex Hardware/Software Platforms. , 2015, , .		24
112	Seeking Time-Composable Partitions of Tasks for COTS Multicore Processors. , 2015, , .		5
113	IEC-61508 SIL 3 Compliant Pseudo-Random Number Generators for Probabilistic Timing Analysis. , 2015, , .		15
114	Timely Error Detection for Effective Recovery in Light-Lockstep Automotive Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1718-1729.	2.7	23
115	Characterizing fault propagation in safety-critical processor designs. , 2015, , .		3
116	CAP: Communication-Aware Allocation Algorithm for Real-Time Parallel Applications on Many-Cores. , 2015, , .		1
117	Resource usage templates and signatures for COTS multicore processors. , 2015, , .		8
118	WCET analysis methods: Pitfalls and challenges on their trustworthiness. , 2015, , .		65
119	Introduction to partial time composability for COTS multicores. , 2015, , .		3
120	Analysis and RTL correlation of instruction set simulators for automotive microcontroller robustness verification. , 2015, , .		12
121	Increasing confidence on measurement-based contention bounds for real-time round-robin buses. , 2015, , .		12
122	PACO. , 2015, , .		0
123	Speeding up Static Probabilistic Timing Analysis. Lecture Notes in Computer Science, 2015, , 236-247.	1.3	4
124	A Dual-Criticality Memory Controller (DCmc): Proposal and Evaluation of a Space Case Study. , 2014, , .		36
125	Hybrid Cache Designs for Reliable Hybrid High and Ultra-Low Voltage Operation. ACM Transactions on Design Automation of Electronic Systems, 2014, 20, 1-25.	2.6	1
126	Measurement-Based Probabilistic Timing Analysis and Its Impact on Processor Architecture. , 2014, , .		20

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127	RunPar. , 2014, , .		27
128	PUB: Path Upper-Bounding for Measurement-Based Probabilistic Timing Analysis. , 2014, , .		16
129	On the Comparison of Deterministic and Probabilistic WCET Estimation Techniques. , 2014, , .		46
130	LiVe. , 2014, , .		6
131	Time-Analysable Non-Partitioned Shared Caches for Real-Time Multicore Systems. , 2014, , .		19
132	Per-task Energy Accounting in Computing Systems. IEEE Computer Architecture Letters, 2014, 13, 85-88.	1.5	4
133	AHRB: A high-performance time-composable AMBA AHB bus. , 2014, , .		6
134	Parallel many-core avionics systems. , 2014, , .		8
135	Timing Verification of Fault-Tolerant Chips for Safety-Critical Applications in Harsh Environments. IEEE Micro, 2014, 34, 8-19.	1.8	10
136	Bus designs for time-probabilistic multicore processors. , 2014, , .		15
137	Containing Timing-Related Certification Cost in Automotive Systems Deploying Complex Hardware. , 2014, , .		15
138	Heart of Gold: Making the Improbable Happen to Increase Confidence in MBPTA. , 2014, , .		23
139	Analyzing the Efficiency of L1 Caches for Reliable Hybrid-Voltage Operation Using EDC Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2211-2215.	3.1	1
140	Efficient Cache Designs for Probabilistically Analysable Real-Time Systems. IEEE Transactions on Computers, 2014, 63, 2998-3011.	3.4	12
141	Bus designs for time-probabilistic multicore processors. , 2014, , .		7
142	DReAM: Per-Task DRAM Energy Metering in Multicore Systems. Lecture Notes in Computer Science, 2014, , 111-123.	1.3	1
143	DTM: Degraded Test Mode for Fault-Aware Probabilistic Timing Analysis. , 2013, , .		20
144	A Cache Design for Probabilistically Analysable Real-time Systems. , 2013, , .		48

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145	Efficient Cache Architectures for Reliable Hybrid Voltage Operation Using EDC Codes. , 2013, , .		4
146	Deconstructing bus access control policies for Real-Time multicores. , 2013, , .		20
147	Multi-level Unified Caches for Probabilistically Time Analysable Real-Time Systems. , 2013, , .		21
148	Probabilistic Timing Analysis on Conventional Cache Designs. , 2013, , .		19
149	Implicit-storing and redundant-encoding-of-attribute information in error-correction-codes. , 2013, , .		6
150	APPLE. , 2013, , .		5
151	On the convergence of mainstream and mission-critical markets. , 2013, , .		6
152	Hardware support for accurate per-task energy metering in multicore systems. Transactions on Architecture and Code Optimization, 2013, 10, 1-27.	2.0	10
153	Achieving timing composability with measurement-based probabilistic timing analysis. , 2013, , .		11
154	Supporting industrial use of probabilistic timing analysis with explicit argumentation. , 2013, , .		11
155	Measurement-based probabilistic timing analysis: Lessons from an integrated-modular avionics case study. , 2013, , .		50
156	parMERASA -- Multi-core Execution of Parallelised Hard Real-Time Applications Supporting Analysability. , 2013, , .		34
157	PROARTIS. Transactions on Embedded Computing Systems, 2013, 12, 1-26.	2.9	89
158	On-chip ring network designs for hard-real time systems. , 2013, , .		6
159	Hardware support for accurate per-task energy metering in multicore systems. Transactions on Architecture and Code Optimization, 2013, 10, 1-27.	2.0	3
160	ADAM. , 2012, , .		6
161	Measurement-Based Probabilistic Timing Analysis for Multi-path Programs. , 2012, , .		159
162	Hardware/software-based diagnosis of load-store queues using expandable activity logs. , 2011, , .		4

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163	Fast time-to-market with via-configurable transistor array regular fabric: A delay-locked loop design case study. , 2011, , .		3
164	RVC-based time-predictable faulty caches for safety-critical systems. , 2011, , .		9
165	Implementing End-to-End Register Data-Flow Continuous Self-Test. IEEE Transactions on Computers, 2011, 60, 1194-1206.	3.4	2
166	Hybrid high-performance low-power and ultra-low energy reliable caches. , 2011, , .		5
167	Control-Flow Recovery Validation Using Microarchitectural Invariants. , 2011, , .		0
168	Towards improved survivability in safety-critical systems. , 2011, , .		14
169	Design of complex circuits using the Via-Configurable transistor array regular layout fabric. , 2011, , .		0
170	RVC. , 2011, , .		12
171	Exploiting intra-task slack time of load operations for DVFS in hard real-time multi-core systems. ACM SIGBED Review, 2011, 8, 32-35.	1.8	5
172	Compiler Directed Issue Queue Energy Reduction. Lecture Notes in Computer Science, 2011, , 42-62.	1.3	0
173	VCTA: A Via-Configurable Transistor Array regular fabric. , 2010, , .		11
174	Electromigration for microarchitects. ACM Computing Surveys, 2010, 42, 1-18.	23.0	20
175	Microarchitectural Online Testing for Failure Detection in Memory Order Buffers. IEEE Transactions on Computers, 2010, 59, 623-637.	3.4	10
176	High-Performance low-vcc in-order core. , 2010, , .		3
177	Exploring the limits of early register release. Transactions on Architecture and Code Optimization, 2009, 6, 1-30.	2.0	9
178	Selective replication. ACM Transactions on Computer Systems, 2009, 27, 1-30.	0.8	25
179	Energy-efficient register caching with compiler assistance. Transactions on Architecture and Code Optimization, 2009, 6, 1-23.	2.0	18
180	Low Vccmin fault-tolerant cache with highly predictable performance. , 2009, , .		63

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181	Online error detection and correction of erratic bits in register files. , 2009, , .		4
182	End-to-end register data-flow continuous self-test. Computer Architecture News, 2009, 37, 105-115.	2.5	3
183	End-to-end register data-flow continuous self-test. , 2009, , .		12
184	Refueling: Preventing Wire Degradation due to Electromigration. IEEE Micro, 2008, 28, 37-46.	1.8	19
185	Issue system protection mechanisms. , 2008, , .		3
186	On-Line Failure Detection and Confinement in Caches. , 2008, , .		15
187	On-line Failure Detection in Memory Order Buffers. , 2008, , .		5
188	Fuse: A Technique to Anticipate Failures due to Degradation in ALUs. , 2007, , .		6
189	Penelope: The NBTI-Aware Processor. , 2007, , .		138
190	Surviving to Errors in Multi-Core Environments. , 2007, , .		0
191	SAMIE-LSQ: set-associative multiple-instruction entry load/store queue. , 2006, , .		2
192	Heterogeneous way-size cache. , 2006, , .		21
193	An accurate cost model for guiding data locality transformations. ACM Transactions on Programming Languages and Systems, 2005, 27, 946-987.	2.1	3
194	IATAC: a smart predictor to turn-off L2 cache lines. Transactions on Architecture and Code Optimization, 2005, 2, 55-77.	2.0	76
195	Variable-based multi-module data caches for clustered VLIW processors. , 2005, , .		3
196	Compiler directed early register release. , 2005, , .		26
197	Power- and complexity-aware issue queue designs. IEEE Micro, 2003, 23, 50-58.	1.8	22
198	Power-Aware Adaptive Issue Queue and Register File. Lecture Notes in Computer Science, 2003, , 34-43.	1.3	5

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199	Near-optimal loop tiling by means of cache miss equations and genetic algorithms. , 0, , .		8
200	Inherently Workload-Balanced Clustered Microarchitecture. , 0, , .		2
201	ADBench: benchmarking autonomous driving systems. Computing (Vienna/New York), 0, , 1.	4.8	1
202	Dissecting Robust Resource Partitioning, Robust Time Partitioning, and Robust Partitioning in CAST-32A. , 0, , .		2