Changsik Yoo

List of Publications by Year in Descending Order

77 papers	833 citations	16 h-index	26 g-index
87 ext. papers	1,034 ext. citations	3.1 avg, IF	4.21 L-index

#	Paper	IF	Citations
77	Digital Low-Dropout Regulator with Voltage-Controlled Oscillator Based Control. *IEEE Transactions on Power Electronics*, **2021**, 1-1	7.2	1
76	Solar Energy-Harvesting Buck–Boost Converter With Battery-Charging and Battery-Assisted Modes. *IEEE Transactions on Industrial Electronics*, **2021**, 68, 2163-2172	8.9	1
75	A 6-Gb/s Wireline Receiver With Intrapair Skew Compensation and Three-Tap Decision-Feedback Equalizer in 28-nm CMOS. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 1107-1117	2.6	2
74	Voltage-mode PAM4 driver with differential ternary R-2R DAC architecture. *Electronics Letters*, **2020**, 56, 431-432	1.1	1
73	Time-Domain Operational Amplifier With Voltage-Controlled Oscillator and Its Application to Active-RC Analog Filter. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 415-419	3.5	6
72	A Time-Domain-Controlled Current-Mode Buck Converter With Wide Output Voltage Range. *IEEE Journal of Solid-State Circuits*, **2019**, 54, 865-873	5.5	13
71	A 4-MHz Bandwidth Continuous-Time Sigma-Delta Modulator With Stochastic Quantizer and Digital Accumulator. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2019**, 66, 1124-1128	3.5	2
70	A Current-Mode Hysteretic Buck Converter With Multiple-Reset RC-Based Inductor Current Sensor. *IEEE Transactions on Industrial Electronics*, **2019**, 66, 8445-8453	8.9	10
69	A Non-Volatile Ternary Content-Addressable Memory Cell for Low-Power and Variation-Toleration Operation. *IEEE Transactions on Magnetics*, **2018**, 54, 1-3	2	7
68	Continuous-time linear equalizer with automatic boosting gain adaptation and input offset cancellation. *International Journal of Circuit Theory and Applications*, **2018**, 46, 2151-2159	2	1
67	A 12-Gb/s HDMI 2.1 quarter-rate transmitter in 28-nm bulk CMOS process. *Analog Integrated Circuits and Signal Processing*, **2018**, 96, 363-370	1.2	
66	A $f_{mathrm{REF}}/5$ Bandwidth Type-II Charge-Pump Phase-Locked Loop With Dual-Edge Phase Comparison and Sampling Loop Filter. *IEEE Microwave and Wireless Components Letters*, **2018**, 28, 825-827	2.6	3
65	A simultaneously bidirectional inductively coupled link in a 0.13-μm CMOS technology. *International Journal of Circuit Theory and Applications*, **2017**, 45, 515-529	2	2
64	A Stochastic Flash Analog-to-Digital Converter Linearized by Reference Swapping. *IEEE Access*, **2017**, 5, 23046-23051	3.5	9
63	Switching Battery Charger Integrated Circuit for Mobile Devices in a 130-nm BCDMOS Process. *IEEE Transactions on Power Electronics*, **2016**, 31, 7943-7952	7.2	16
62	Quasi-Resonant (QR) Controller With Adaptive Switching Frequency Reduction Scheme for Flyback Converter. *IEEE Transactions on Industrial Electronics*, **2016**, 63, 3571-3581	8.9	27
61	Wireless power charger for wearable medical devices with in-band communication. *International Journal of Circuit Theory and Applications*, **2016**, 44, 1483-1493	2	7

60	A HDMI-to-MHL video format conversion system-on-chip (SoC) for mobile handset in a 130-nm CMOS technology **2016**,		1
59	Skew cancellation technique for >256-Gbyte/s high-bandwidth memory (HBM). *Electronics Letters*, **2016**, 52, 1155-1157	1.1	2
58	A 6-Gbps/lane receiver for a clock-forwarded link in 65-nm CMOS process. *International Journal of Circuit Theory and Applications*, **2015**, 43, 544-552	2	1
57	A Multiphase Synchronous Buck Converter With a Fully Integrated Current Balancing Scheme. *IEEE Transactions on Power Electronics*, **2015**, 30, 5159-5169	7.2	24
56	A 6-Gbps dual-mode digital clock and data recovery circuit in a 65-nm CMOS technology. *Analog Integrated Circuits and Signal Processing*, **2015**, 85, 209-215	1.2	
55	Variation-Tolerant Sensing Circuit for Spin-Transfer Torque MRAM. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2015**, 62, 1134-1138	3.5	5
54	An analog sigma-delta modulator with shared operational amplifier for low-power class-D audio amplifier. *IEICE Electronics Express*, **2015**, 12, 20150562-20150562	0.5	0
53	A switch-mode boost DC□DC converter for IR-drop compensation of charging cable. *International Journal of Circuit Theory and Applications*, **2015**, 43, 1391-1398	2	3
52	Crosstalk cancelling voltage-mode driver for multi-Gbps parallel DRAM interface. *International Journal of Circuit Theory and Applications*, **2015**, 43, 1175-1182	2	
51	A 5.25-V-tolerant bidirectional I/O circuit in a 28-nm CMOS process. *International Journal of Circuit Theory and Applications*, **2015**, 43, 822-828	2	1
50	A 100-kS/s 8.3-ENOB 1.7- $muhbox{W}$ Time-Domain Analog-to-Digital Converter. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2014**, 61, 408-412	3.5	10
49	A CCM/DCM Dual-Mode Synchronous Rectification Controller for a High-Efficiency Flyback Converter. *IEEE Transactions on Power Electronics*, **2014**, 29, 768-774	7.2	30
48	A digital lock detector for a dual loop PLL **2014**,		3
47	Data and edge decision feedback equalizer with >1.0-UI timing margin for both data and edge samples. *IEICE Electronics Express*, **2014**, 11, 20140274-20140274	0.5	2
46	A 1.5□3.0 Gb/s clock and data recovery circuit with dual-PFD phase-rotating phase locked loop. *IEICE Electronics Express*, **2014**, 11, 20140351-20140351	0.5	2
45	Intra-panel interface with clock-embedded differential signalling for large size digital television. *International Journal of Electronics*, **2014**, 101, 133-142	1.2	
44	A fast automatic frequency calibration technique for a 2□ GHz frequency synthesizer. *International Journal of Circuit Theory and Applications*, **2014**, 42, 309-320	2	2
43	A Two-Phase Interleaved Power Factor Correction Boost Converter With a Variation-Tolerant Phase Shifting Technique. *IEEE Transactions on Power Electronics*, **2014**, 29, 1032-1040	7.2	27

42	Macro-Model of Magnetic Tunnel Junction for STT-MRAM including Dynamic Behavior. *Journal of Semiconductor Technology and Science*, **2014**, 14, 728-732	1.5	6
41	An automatic load-adaptive switching frequency selection technique for improving the light-load efficiency of a buck converter. *Analog Integrated Circuits and Signal Processing*, **2013**, 75, 349-358	1.2	3
40	A 3.4-Gbps clock and data recovery circuit with a forwarded clock in a 0.13-□n CMOS technology. *International Journal of Electronics Letters*, **2013**, 1, 77-86	0.6	
39	A Class-D Amplifier With Pulse Code Modulated (PCM) Digital Input for Digital Hearing Aid. *IEEE Journal of Solid-State Circuits*, **2013**, 48, 465-472	5.5	13
38	Skew Compensation Technique for Source-Synchronous Parallel DRAM Interface. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 2155-2159	2.6	7
37	Load-Independent Current Control Technique of a Single-Inductor Multiple-Output Switching DC□DC converter. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2012**, 59, 50-54	3.5	29
36	Measurement of Intersymbol Interference Jitter by Fractional Oversampling for Adaptive Equalization. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2012**, 59, 716-720	3.5	2
35	A 3.0-W wireless power receiver circuit with 75-% overall efficiency **2012**,		14
34	A 2x2 MIMO Tri-Band Dual-Mode Direct-Conversion CMOS Transceiver for Worldwide WiMAX/WLAN Applications. *IEEE Journal of Solid-State Circuits*, **2011**, 46, 1648-1658	5.5	23
33	A 20-MHz Bandwidth Continuous-Time Sigma-Delta Modulator With Jitter Immunity Improved Full Clock Period SCR (FSCR) DAC and High-Speed DWA. *IEEE Journal of Solid-State Circuits*, **2011**, 46, 2469-2477	5.5	17
32	. *IEEE Transactions on Consumer Electronics*, **2010**, 56, 2032-2036	4.8	10
31	Spread spectrum clock generation for reduced electro-magnetic interference in consumer electronics devices. *IEEE Transactions on Consumer Electronics*, **2010**, 56, 844-847	4.8	9
30	A Direct-Conversion CMOS RF Receiver Reconfigurable From 2 to 6 GHz. *IEEE Transactions on Microwave Theory and Techniques*, **2010**, 58, 2326-2333	4.1	15
29	A 0.6 V, 2.11 MHz, 62 dB SFDR active-RC filter in 0.13□m CMOS process. *International Journal of Circuit Theory and Applications*, **2010**, 38, 99-107	2	2
28	A Fast automatic frequency calibration (AFC) scheme for phase-locked loop (PLL) frequency synthesizer **2009**,		11
27	A 4.39□5.26 GHz LC-Tank CMOS Voltage-Controlled Oscillator With Small VCO-Gain Variation. *IEEE Microwave and Wireless Components Letters*, **2009**, 19, 524-526	2.6	68
26	A 5-Gbit/s Clock- and Data-Recovery Circuit With 1/8-Rate Linear Phase Detector in 0.18- ${rm mu}hbox{m}$ CMOS Technology. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2009**, 56, 6-10	3.5	16
25	An $L1$ -Band Dual-Mode RF Receiver for GPS and Galileo in 0.18-$mu {hbox{m}}$ CMOS. *IEEE Transactions on Microwave Theory and Techniques*, **2009**, 57, 919-927	4.1	25

24	A L1-band dual-mode RF receiver for GPS and Galileo in 0.18μm CMOS **2008**,		1
23	Current Reusing VCO and Divide-by-Two Frequency Divider for Quadrature LO Generation. *IEEE Microwave and Wireless Components Letters*, **2008**, 18, 413-415	2.6	36
22	38.3: All-Digital Phase-Locked Loop with Low-Temperature Poly-Silicon Thin Film Transistor for System-on-Glass. *Digest of Technical Papers SID International Symposium*, **2008**, 39, 549	0.5	
21	Fully-Integrated CMOS Direct-Conversion Receiver for 5GHz Wireless LAN **2007**,		1
20	A CMOS multiphase shifting network with RC-CR filter and bias-level-scaled active interpolator. *Microwave and Optical Technology Letters*, **2007**, 49, 118-121	1.2	1
19	Low-voltage and high-frequency Gm-opamp-C filter with automatic self frequency tuning. *Analog Integrated Circuits and Signal Processing*, **2007**, 50, 285-290	1.2	
18	56.5: High-Speed and Low-Power Analog Source Driver for TFT-LCD Using Dynamic Current Biased Operational Amplifier. *Digest of Technical Papers SID International Symposium*, **2007**, 38, 1647-1650	0.5	6
17	Display System Interface without Line Memory for Low-Cost System-on-Glass. *IEEE Transactions on Consumer Electronics*, **2007**, 53, 1226-1229	4.8	3
16	CMOS current reference with supply and temperature compensation. *Electronics Letters*, **2007**, 43, 1422	1.1	46
15	5-GHz Low-Phase Noise CMOS Quadrature VCO. *IEEE Microwave and Wireless Components Letters*, **2006**, 16, 609-611	2.6	21
14	A low-ripple poly-Si TFT charge pump for driver-integrated LCD panel. *IEEE Transactions on Consumer Electronics*, **2005**, 51, 606-610	4.8	20
13	Digitally controlled phase locked loop with tracking analog-to-digital converter **2005**,		1
12	Open-loop full-digital duty cycle correction circuit. *Electronics Letters*, **2005**, 41, 635	1.1	16
11	Threshold voltage and mobility mismatch compensated analogue buffer for driver-integrated poly-Si TFT LCDs. *Electronics Letters*, **2005**, 41, 65	1.1	9
10	Low-Phase Noise LC-tank Quadrature Voltage Controlled Oscillator **2005**,		1
9	Characteristics of poly-Si TFTs required for System-on-Glass analog circuits. *Journal of Information Display*, **2004**, 5, 1-6	4.1	1
8	A 1.8-V 700-mb/s/pin 512-mb DDR-II SDRAM with on-die termination and off-chip driver calibration. *IEEE Journal of Solid-State Circuits*, **2004**, 39, 941-951	5.5	19
7	A common-gate switched 0.9-W class-E power amplifier with 41% PAE in 0.25-/spl mu/m CMOS. *IEEE Journal of Solid-State Circuits*, **2001**, 36, 823-830	5.5	97

6	A 2.5-V, 333-Mb/s/pin, 1-Gbit, double-data-rate synchronous DRAM. *IEEE Journal of Solid-State Circuits*, **1999**, 34, 1589-1599	5.5	12
5	A /spl plusmn/1.5-V, 4-MHz CMOS continuous-time filter with a single-integrator based tuning. *IEEE Journal of Solid-State Circuits*, **1998**, 33, 18-27	5.5	32
4	. *IEEE Journal of Solid-State Circuits*, **1995**, 30, 616-620	5.5	4
3	A low-power wide-bandwidth fully differential operational amplifier with current re-using feedforward frequency compensation		4
2	Digital delay locked loop with open-loop digital duty cycle corrector for 1.2Gb/s/pin double data rate SDRAM		6
1	Active-RC channel selection filter tunable from 6 kHz to 18 MHz for software-defined radio		3