

Changsik Yoo

List of Publications by Citations

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77
papers

833
citations

16
h-index

26
g-index

87
ext. papers

1,034
ext. citations

3.1
avg, IF

4.21
L-index

#	Paper	IF	Citations
77	A common-gate switched 0.9-W class-E power amplifier with 41% PAE in 0.25- μm CMOS. <i>IEEE Journal of Solid-State Circuits</i> , 2001 , 36, 823-830	5.5	97
76	A 4.398.26 GHz LC-Tank CMOS Voltage-Controlled Oscillator With Small VCO-Gain Variation. <i>IEEE Microwave and Wireless Components Letters</i> , 2009 , 19, 524-526	2.6	68
75	CMOS current reference with supply and temperature compensation. <i>Electronics Letters</i> , 2007 , 43, 1422-1424	1.1	46
74	Current Reusing VCO and Divide-by-Two Frequency Divider for Quadrature LO Generation. <i>IEEE Microwave and Wireless Components Letters</i> , 2008 , 18, 413-415	2.6	36
73	A ± 1.5 -V, 4-MHz CMOS continuous-time filter with a single-integrator based tuning. <i>IEEE Journal of Solid-State Circuits</i> , 1998 , 33, 18-27	5.5	32
72	A CCM/DCM Dual-Mode Synchronous Rectification Controller for a High-Efficiency Flyback Converter. <i>IEEE Transactions on Power Electronics</i> , 2014 , 29, 768-774	7.2	30
71	Load-Independent Current Control Technique of a Single-Inductor Multiple-Output Switching DC/DC converter. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2012 , 59, 50-54	3.5	29
70	Quasi-Resonant (QR) Controller With Adaptive Switching Frequency Reduction Scheme for Flyback Converter. <i>IEEE Transactions on Industrial Electronics</i> , 2016 , 63, 3571-3581	8.9	27
69	A Two-Phase Interleaved Power Factor Correction Boost Converter With a Variation-Tolerant Phase Shifting Technique. <i>IEEE Transactions on Power Electronics</i> , 2014 , 29, 1032-1040	7.2	27
68	An L_1 -Band Dual-Mode RF Receiver for GPS and Galileo in 0.18- μm CMOS. <i>IEEE Transactions on Microwave Theory and Techniques</i> , 2009 , 57, 919-927	4.1	25
67	A Multiphase Synchronous Buck Converter With a Fully Integrated Current Balancing Scheme. <i>IEEE Transactions on Power Electronics</i> , 2015 , 30, 5159-5169	7.2	24
66	A 2x2 MIMO Tri-Band Dual-Mode Direct-Conversion CMOS Transceiver for Worldwide WiMAX/WLAN Applications. <i>IEEE Journal of Solid-State Circuits</i> , 2011 , 46, 1648-1658	5.5	23
65	5-GHz Low-Phase Noise CMOS Quadrature VCO. <i>IEEE Microwave and Wireless Components Letters</i> , 2006 , 16, 609-611	2.6	21
64	A low-ripple poly-Si TFT charge pump for driver-integrated LCD panel. <i>IEEE Transactions on Consumer Electronics</i> , 2005 , 51, 606-610	4.8	20
63	A 1.8-V 700-Mb/s/pin 512-Mb DDR-II SDRAM with on-die termination and off-chip driver calibration. <i>IEEE Journal of Solid-State Circuits</i> , 2004 , 39, 941-951	5.5	19
62	A 20-MHz Bandwidth Continuous-Time Sigma-Delta Modulator With Jitter Immunity Improved Full Clock Period SCR (FSCR) DAC and High-Speed DWA. <i>IEEE Journal of Solid-State Circuits</i> , 2011 , 46, 2469-2477	5.5	17
61	Switching Battery Charger Integrated Circuit for Mobile Devices in a 130-nm BCDMOS Process. <i>IEEE Transactions on Power Electronics</i> , 2016 , 31, 7943-7952	7.2	16

60	A 5-Gbit/s Clock- and Data-Recovery Circuit With 1/8-Rate Linear Phase Detector in 0.18- μm CMOS Technology. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2009 , 56, 6-10	3.5	16
59	Open-loop full-digital duty cycle correction circuit. <i>Electronics Letters</i> , 2005 , 41, 635	1.1	16
58	A Direct-Conversion CMOS RF Receiver Reconfigurable From 2 to 6 GHz. <i>IEEE Transactions on Microwave Theory and Techniques</i> , 2010 , 58, 2326-2333	4.1	15
57	A 3.0-W wireless power receiver circuit with 75-% overall efficiency 2012 ,		14
56	A Class-D Amplifier With Pulse Code Modulated (PCM) Digital Input for Digital Hearing Aid. <i>IEEE Journal of Solid-State Circuits</i> , 2013 , 48, 465-472	5.5	13
55	A Time-Domain-Controlled Current-Mode Buck Converter With Wide Output Voltage Range. <i>IEEE Journal of Solid-State Circuits</i> , 2019 , 54, 865-873	5.5	13
54	A 2.5-V, 333-Mb/s/pin, 1-Gbit, double-data-rate synchronous DRAM. <i>IEEE Journal of Solid-State Circuits</i> , 1999 , 34, 1589-1599	5.5	12
53	A Fast automatic frequency calibration (AFC) scheme for phase-locked loop (PLL) frequency synthesizer 2009 ,		11
52	A 100-kS/s 8.3-ENOB 1.7- μW Time-Domain Analog-to-Digital Converter. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2014 , 61, 408-412	3.5	10
51	. <i>IEEE Transactions on Consumer Electronics</i> , 2010 , 56, 2032-2036	4.8	10
50	A Current-Mode Hysteretic Buck Converter With Multiple-Reset RC-Based Inductor Current Sensor. <i>IEEE Transactions on Industrial Electronics</i> , 2019 , 66, 8445-8453	8.9	10
49	A Stochastic Flash Analog-to-Digital Converter Linearized by Reference Swapping. <i>IEEE Access</i> , 2017 , 5, 23046-23051	3.5	9
48	Spread spectrum clock generation for reduced electro-magnetic interference in consumer electronics devices. <i>IEEE Transactions on Consumer Electronics</i> , 2010 , 56, 844-847	4.8	9
47	Threshold voltage and mobility mismatch compensated analogue buffer for driver-integrated poly-Si TFT LCDs. <i>Electronics Letters</i> , 2005 , 41, 65	1.1	9
46	A Non-Volatile Ternary Content-Addressable Memory Cell for Low-Power and Variation-Toleration Operation. <i>IEEE Transactions on Magnetics</i> , 2018 , 54, 1-3	2	7
45	Skew Compensation Technique for Source-Synchronous Parallel DRAM Interface. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2013 , 21, 2155-2159	2.6	7
44	Wireless power charger for wearable medical devices with in-band communication. <i>International Journal of Circuit Theory and Applications</i> , 2016 , 44, 1483-1493	2	7
43	56.5: High-Speed and Low-Power Analog Source Driver for TFT-LCD Using Dynamic Current Biased Operational Amplifier. <i>Digest of Technical Papers SID International Symposium</i> , 2007 , 38, 1647-1650	0.5	6

42	Digital delay locked loop with open-loop digital duty cycle corrector for 1.2Gb/s/pin double data rate SDRAM		6
41	Macro-Model of Magnetic Tunnel Junction for STT-MRAM including Dynamic Behavior. <i>Journal of Semiconductor Technology and Science</i> , 2014 , 14, 728-732	1.5	6
40	Time-Domain Operational Amplifier With Voltage-Controlled Oscillator and Its Application to Active-RC Analog Filter. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2020 , 67, 415-419	3.5	6
39	Variation-Tolerant Sensing Circuit for Spin-Transfer Torque MRAM. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2015 , 62, 1134-1138	3.5	5
38	A low-power wide-bandwidth fully differential operational amplifier with current re-using feedforward frequency compensation		4
37	. <i>IEEE Journal of Solid-State Circuits</i> , 1995 , 30, 616-620	5.5	4
36	A digital lock detector for a dual loop PLL 2014 ,		3
35	An automatic load-adaptive switching frequency selection technique for improving the light-load efficiency of a buck converter. <i>Analog Integrated Circuits and Signal Processing</i> , 2013 , 75, 349-358	1.2	3
34	A switch-mode boost DCDC converter for IR-drop compensation of charging cable. <i>International Journal of Circuit Theory and Applications</i> , 2015 , 43, 1391-1398	2	3
33	Display System Interface without Line Memory for Low-Cost System-on-Glass. <i>IEEE Transactions on Consumer Electronics</i> , 2007 , 53, 1226-1229	4.8	3
32	Active-RC channel selection filter tunable from 6 kHz to 18 MHz for software-defined radio		3
31	A $\frac{1}{5}$ Bandwidth Type-II Charge-Pump Phase-Locked Loop With Dual-Edge Phase Comparison and Sampling Loop Filter. <i>IEEE Microwave and Wireless Components Letters</i> , 2018 , 28, 825-827 ^{2,6}		3
30	A 6-Gb/s Wireline Receiver With Intrapair Skew Compensation and Three-Tap Decision-Feedback Equalizer in 28-nm CMOS. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2020 , 28, 1107-1117 ^{2,6}		2
29	Data and edge decision feedback equalizer with >1.0-UI timing margin for both data and edge samples. <i>IEICE Electronics Express</i> , 2014 , 11, 20140274-20140274	0.5	2
28	A 1.5B.0 Gb/s clock and data recovery circuit with dual-PFD phase-rotating phase locked loop. <i>IEICE Electronics Express</i> , 2014 , 11, 20140351-20140351	0.5	2
27	A simultaneously bidirectional inductively coupled link in a 0.13- μ m CMOS technology. <i>International Journal of Circuit Theory and Applications</i> , 2017 , 45, 515-529	2	2
26	A fast automatic frequency calibration technique for a 2B GHz frequency synthesizer. <i>International Journal of Circuit Theory and Applications</i> , 2014 , 42, 309-320	2	2
25	Measurement of Intersymbol Interference Jitter by Fractional Oversampling for Adaptive Equalization. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2012 , 59, 716-720	3.5	2

24	A 0.6 V, 2.11 MHz, 62 dB SFDR active-RC filter in 0.13 μ m CMOS process. <i>International Journal of Circuit Theory and Applications</i> , 2010 , 38, 99-107	2	2
23	Skew cancellation technique for >256-Gbyte/s high-bandwidth memory (HBM). <i>Electronics Letters</i> , 2016 , 52, 1155-1157	1.1	2
22	A 4-MHz Bandwidth Continuous-Time Sigma-Delta Modulator With Stochastic Quantizer and Digital Accumulator. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2019 , 66, 1124-1128	3.5	2
21	A 6-Gbps/lane receiver for a clock-forwarded link in 65-nm CMOS process. <i>International Journal of Circuit Theory and Applications</i> , 2015 , 43, 544-552	2	1
20	Voltage-mode PAM4 driver with differential ternary R-2R DAC architecture. <i>Electronics Letters</i> , 2020 , 56, 431-432	1.1	1
19	Continuous-time linear equalizer with automatic boosting gain adaptation and input offset cancellation. <i>International Journal of Circuit Theory and Applications</i> , 2018 , 46, 2151-2159	2	1
18	A 5.25-V-tolerant bidirectional I/O circuit in a 28-nm CMOS process. <i>International Journal of Circuit Theory and Applications</i> , 2015 , 43, 822-828	2	1
17	A L1-band dual-mode RF receiver for GPS and Galileo in 0.18 μ m CMOS 2008 ,		1
16	Fully-Integrated CMOS Direct-Conversion Receiver for 5GHz Wireless LAN 2007 ,		1
15	A CMOS multiphase shifting network with RC-CR filter and bias-level-scaled active interpolator. <i>Microwave and Optical Technology Letters</i> , 2007 , 49, 118-121	1.2	1
14	Digitally controlled phase locked loop with tracking analog-to-digital converter 2005 ,		1
13	Characteristics of poly-Si TFTs required for System-on-Glass analog circuits. <i>Journal of Information Display</i> , 2004 , 5, 1-6	4.1	1
12	Low-Phase Noise LC-tank Quadrature Voltage Controlled Oscillator 2005 ,		1
11	Digital Low-Dropout Regulator with Voltage-Controlled Oscillator Based Control. <i>IEEE Transactions on Power Electronics</i> , 2021 , 1-1	7.2	1
10	A HDMI-to-MHL video format conversion system-on-chip (SoC) for mobile handset in a 130-nm CMOS technology 2016 ,		1
9	Solar Energy-Harvesting BuckBoost Converter With Battery-Charging and Battery-Assisted Modes. <i>IEEE Transactions on Industrial Electronics</i> , 2021 , 68, 2163-2172	8.9	1
8	An analog sigma-delta modulator with shared operational amplifier for low-power class-D audio amplifier. <i>IEICE Electronics Express</i> , 2015 , 12, 20150562-20150562	0.5	0
7	A 6-Gbps dual-mode digital clock and data recovery circuit in a 65-nm CMOS technology. <i>Analog Integrated Circuits and Signal Processing</i> , 2015 , 85, 209-215	1.2	

- 6 A 12-Gb/s HDMI 2.1 quarter-rate transmitter in 28-nm bulk CMOS process. *Analog Integrated Circuits and Signal Processing*, **2018**, 96, 363-370 1.2
- 5 A 3.4-Gbps clock and data recovery circuit with a forwarded clock in a 0.13- μm CMOS technology. *International Journal of Electronics Letters*, **2013**, 1, 77-86 0.6
- 4 Crosstalk cancelling voltage-mode driver for multi-Gbps parallel DRAM interface. *International Journal of Circuit Theory and Applications*, **2015**, 43, 1175-1182 2
- 3 Intra-panel interface with clock-embedded differential signalling for large size digital television. *International Journal of Electronics*, **2014**, 101, 133-142 1.2
- 2 38.3: All-Digital Phase-Locked Loop with Low-Temperature Poly-Silicon Thin Film Transistor for System-on-Glass. *Digest of Technical Papers SID International Symposium*, **2008**, 39, 549 0.5
- 1 Low-voltage and high-frequency Gm-opamp-C filter with automatic self frequency tuning. *Analog Integrated Circuits and Signal Processing*, **2007**, 50, 285-290 1.2