Changsik Yoo

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/1411056/publications.pdf

Version: 2024-02-01

87 papers	1,232 citations	361296 20 h-index	414303 32 g-index
87 all docs	87 docs citations	87 times ranked	1024 citing authors

#	Article	IF	Citations
1	Digital Low-Dropout Regulator With Voltage-Controlled Oscillator Based Control. IEEE Transactions on Power Electronics, 2022, 37, 6951-6961.	5.4	11
2	A 16Gb 9.5Gb/S/pin LPDDR5X SDRAM With Low-Power Schemes Exploiting Dynamic Voltage-Frequency Scaling and Offset-Calibrated Readout Sense Amplifiers in a Fourth Generation 10nm DRAM Process. , 2022, , .		4
3	Solar Energy-Harvesting Buckâ€"Boost Converter With Battery-Charging and Battery-Assisted Modes. IEEE Transactions on Industrial Electronics, 2021, 68, 2163-2172.	5.2	11
4	A Reflection and Crosstalk Canceling Continuous-Time Linear Equalizer for High-Speed DDR SDRAM. , 2021, , .		4
5	A 3.2-12.8Gb/s Duty-Cycle Compensating Quadrature Error Corrector for DRAM Interfaces, With Fast Locking and Low Power Characteristics. , 2021, , .		4
6	Time-Domain Operational Amplifier With Voltage-Controlled Oscillator and Its Application to Active-RC Analog Filter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 415-419.	2.2	12
7	A 6-Gb/s Wireline Receiver With Intrapair Skew Compensation and Three-Tap Decision-Feedback Equalizer in 28-nm CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1107-1117.	2.1	3
8	Voltageâ€mode PAM4 driver with differential ternary Râ€2R DAC architecture. Electronics Letters, 2020, 56, 431-432.	0.5	1
9	A Time-Domain-Controlled Current-Mode Buck Converter With Wide Output Voltage Range. IEEE Journal of Solid-State Circuits, 2019, 54, 865-873.	3.5	29
10	A 4-MHz Bandwidth Continuous-Time Sigma-Delta Modulator With Stochastic Quantizer and Digital Accumulator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1124-1128.	2.2	3
11	A Current-Mode Hysteretic Buck Converter With Multiple-Reset RC-Based Inductor Current Sensor. IEEE Transactions on Industrial Electronics, 2019, 66, 8445-8453.	5.2	13
12	A Non-Volatile Ternary Content-Addressable Memory Cell for Low-Power and Variation-Toleration Operation. IEEE Transactions on Magnetics, 2018, 54, 1-3.	1.2	12
13	A <inline-formula> <tex-math notation="LaTeX">$f_{mathrm{REF}}/5$ </tex-math> </inline-formula> Bandwidth Type-II Charge-Pump Phase-Locked Loop With Dual-Edge Phase Comparison and Sampling Loop Filter. IEEE Microwave and Wireless Components Letters, 2018, 28, 825-827.	2.0	8
14	Continuousâ€time linear equalizer with automatic boosting gain adaptation and input offset cancellation. International Journal of Circuit Theory and Applications, 2018, 46, 2151-2159.	1.3	1
15	A 12-Gb/s HDMI 2.1 quarter-rate transmitter in 28-nm bulk CMOS process. Analog Integrated Circuits and Signal Processing, 2018, 96, 363-370.	0.9	0
16	A simultaneously bidirectional inductively coupled link in a 0.13â€Âµm CMOS technology. International Journal of Circuit Theory and Applications, 2017, 45, 515-529.	1.3	2
17	A Stochastic Flash Analog-to-Digital Converter Linearized by Reference Swapping. IEEE Access, 2017, 5, 23046-23051.	2.6	18
18	Wireless power charger for wearable medical devices with inâ€band communication. International Journal of Circuit Theory and Applications, 2016, 44, 1483-1493.	1.3	9

#	Article	IF	Citations
19	A HDMI-to-MHL video format conversion system-on-chip (SoC) for mobile handset in a 130-nm CMOS technology. , 2016, , .		1
20	Skew cancellation technique for >256â€Gbyte/s highâ€bandwidth memory (HBM). Electronics Letters, 2016, 52, 1155-1157.	0.5	3
21	Switching Battery Charger Integrated Circuit for Mobile Devices in a 130-nm BCDMOS Process. IEEE Transactions on Power Electronics, 2016, 31, 7943-7952.	5.4	29
22	Quasi-Resonant (QR) Controller With Adaptive Switching Frequency Reduction Scheme for Flyback Converter. IEEE Transactions on Industrial Electronics, 2016, 63, 3571-3581.	5.2	41
23	An analog sigma-delta modulator with shared operational amplifier for low-power class-D audio amplifier. IEICE Electronics Express, 2015, 12, 20150562-20150562.	0.3	1
24	A switchâ€mode boost DCâ€“DC converter for IRâ€drop compensation of charging cable. International Journal of Circuit Theory and Applications, 2015, 43, 1391-1398.	1.3	3
25	Crosstalk cancelling voltage-mode driver for multi-Gbps parallel DRAM interface. International Journal of Circuit Theory and Applications, 2015, 43, 1175-1182.	1.3	1
26	A 5.25-V-tolerant bidirectional I/O circuit in a 28-nm CMOS process. International Journal of Circuit Theory and Applications, 2015, 43, 822-828.	1.3	1
27	A 6â€Gbps/lane receiver for a clockâ€forwarded link in 65â€nm CMOS process. International Journal of Circuit Theory and Applications, 2015, 43, 544-552.	1.3	1
28	A Multiphase Synchronous Buck Converter With a Fully Integrated Current Balancing Scheme. IEEE Transactions on Power Electronics, 2015, 30, 5159-5169.	5.4	41
29	A 6-Gbps dual-mode digital clock and data recovery circuit in a 65-nm CMOS technology. Analog Integrated Circuits and Signal Processing, 2015, 85, 209-215.	0.9	0
30	Variation-Tolerant Sensing Circuit for Spin-Transfer Torque MRAM. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 1134-1138.	2.2	6
31	Intra-panel interface with clock-embedded differential signalling for large size digital television. International Journal of Electronics, 2014, 101, 133-142.	0.9	0
32	A fast automatic frequency calibration technique for a 2â€“6â€‰GHz frequency synthesizer. International Journal of Circuit Theory and Applications, 2014, 42, 309-320.	1.3	3
33	A Two-Phase Interleaved Power Factor Correction Boost Converter With a Variation-Tolerant Phase Shifting Technique. IEEE Transactions on Power Electronics, 2014, 29, 1032-1040.	5.4	34
34	A 100-kS/s 8.3-ENOB 1.7-<named-content content-type="math" xlink:type="simple"> <inline-formula> <tex-math notation="TeX">$muhbox{W}$</tex-math></inline-formula></named-content> Time-Domain Analog-to-Digital Converter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 408-412.	2.2	13
35	A CCM/DCM Dual-Mode Synchronous Rectification Controller for a High-Efficiency Flyback Converter. IEEE Transactions on Power Electronics, 2014, 29, 768-774.	5.4	45
36	A digital lock detector for a dual loop PLL. , 2014, , .		3

#	Article	IF	Citations
37	Data and edge decision feedback equalizer with >1.0-UI timing margin for both data and edge samples. IEICE Electronics Express, 2014, 11, 20140274-20140274.	0.3	2
38	A 1.5â€“5.0 Gb/s clock and data recovery circuit with dual-PFD phase-rotating phase locked loop. IEICE Electronics Express, 2014, 11, 20140351-20140351.	0.3	3
39	Macro-Model of Magnetic Tunnel Junction for STT-MRAM including Dynamic Behavior. Journal of Semiconductor Technology and Science, 2014, 14, 728-732.	0.1	6
40	An automatic load-adaptive switching frequency selection technique for improving the light-load efficiency of a buck converter. Analog Integrated Circuits and Signal Processing, 2013, 75, 349-358.	0.9	3
41	A 3.4-Gbps clock and data recovery circuit with a forwarded clock in a 0.13-Î¼m CMOS technology. International Journal of Electronics Letters, 2013, 1, 77-86.	0.7	0
42	A Class-D Amplifier With Pulse Code Modulated (PCM) Digital Input for Digital Hearing Aid. IEEE Journal of Solid-State Circuits, 2013, 48, 465-472.	3.5	17
43	Skew Compensation Technique for Source-Synchronous Parallel DRAM Interface. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 2155-2159.	2.1	7
44	High efficient power receiver IC with load modulator for wireless resonant power transfer. , 2012, , .		0
45	Measurement of Intersymbol Interference Jitter by Fractional Oversampling for Adaptive Equalization. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 716-720.	2.2	2
46	A 3.0-W wireless power receiver circuit with 75-% overall efficiency. , 2012, , .		21
47	Load-Independent Current Control Technique of a Single-Inductor Multiple-Output Switching DCâ€“DC converter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 50-54.	2.2	32
48	A 2x2 MIMO Tri-Band Dual-Mode Direct-Conversion CMOS Transceiver for Worldwide WiMAX/WLAN Applications. IEEE Journal of Solid-State Circuits, 2011, 46, 1648-1658.	3.5	31
49	A 20-MHz Bandwidth Continuous-Time Sigma-Delta Modulator With Jitter Immunity Improved Full Clock Period SCR (FSCR) DAC and High-Speed DWA. IEEE Journal of Solid-State Circuits, 2011, 46, 2469-2477.	3.5	21
50	Spread spectrum clock generation for reduced electro-magnetic interference in consumer electronics devices. IEEE Transactions on Consumer Electronics, 2010, 56, 844-847.	3.0	12
51	A Direct-Conversion CMOS RF Receiver Reconfigurable From 2 to 6 GHz. IEEE Transactions on Microwave Theory and Techniques, 2010, 58, 2326-2333.	2.9	20
52	A 0.6â€‰V, 2.11â€‰MHz, 62â€‰dB SFDR activeâ€RC filter in 0.13Âµm CMOS process. International Journal of Circuit Theory and Applications, 2010, 38, 99-107.	1.3	2
53	A 1.62/2.7Gbps clock and data recovery with pattern based frequency detector for displayport. IEEE Transactions on Consumer Electronics, 2010, 56, 2032-2036.	3.0	11
54	A 20MHz bandwidth continuous-time. , 2010, , .		3

#	Article	IF	Citations
55	A 2×2 MIMO tri-band dual-mode CMOS transceiver for worldwide WiMAX/WLAN applications. , 2010, , .		4
56	A Fast automatic frequency calibration (AFC) scheme for phase-locked loop (PLL) frequency synthesizer. , 2009, , .		16
57	A 4.39â€"5.26 GHz LC-Tank CMOS Voltage-Controlled Oscillator With Small VCO-Gain Variation. IEEE Microwave and Wireless Components Letters, 2009, 19, 524-526.	2.0	96
58	A 5-Gbit/s Clock- and Data-Recovery Circuit With 1/8-Rate Linear Phase Detector in 0.18-${m mu}hbox{m}$ CMOS Technology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 6-10.	2.2	23
59	An $L1$-Band Dual-Mode RF Receiver for GPS and Galileo in 0.18-$mu {hbox{m}}$ CMOS. IEEE Transactions on Microwave Theory and Techniques, 2009, 57, 919-927.	2.9	29
60	A L1-band dual-mode RF receiver for GPS and Galileo in 0.18μm CMOS. , 2008, , .		2
61	Current Reusing VCO and Divide-by-Two Frequency Divider for Quadrature LO Generation. IEEE Microwave and Wireless Components Letters, 2008, 18, 413-415.	2.0	42
62	A direct-conversion CMOS RF receiver reconfigurable from 2GHz to 6GHz. , 2008, , .		2
63	Low voltage analog digital converter using sigma-delta modulator. , 2008, , .		1
64	38.3: All-Digital Phase-Locked Loop with Low-Temperature Poly-Silicon Thin Film Transistor for System-on-Glass. Digest of Technical Papers SID International Symposium, 2008, 39, 549.	0.1	0
65	56.5: High-Speed and Low-Power Analog Source Driver for TFT-LCD Using Dynamic Current Biased Operational Amplifier. Digest of Technical Papers SID International Symposium, 2007, 38, 1647-1650.	0.1	6
66	Display System Interface without Line Memory for Low-Cost System-on-Glass. IEEE Transactions on Consumer Electronics, 2007, 53, 1226-1229.	3.0	5
67	CMOS current reference with supply and temperature compensation. Electronics Letters, 2007, 43, 1422.	0.5	68
68	Fully-Integrated CMOS Direct-Conversion Receiver for 5GHz Wireless LAN. , 2007, , .		2
69	A CMOS multiphase shifting network with RC-CR filter and bias-level-scaled active interpolator. Microwave and Optical Technology Letters, 2007, 49, 118-121.	0.9	1
70	Low-voltage and high-frequency Gm-opamp-C filter with automatic self frequency tuning. Analog Integrated Circuits and Signal Processing, 2007, 50, 285-290.	0.9	0
71	5-GHz Low-Phase Noise CMOS Quadrature VCO. IEEE Microwave and Wireless Components Letters, 2006, 16, 609-611.	2.0	34
72	A Full-Digital Multi-Channel CMOS Capacitive Sensor. , 2006, , .		2

#	Article	IF	Citations
73	Threshold voltage and mobility mismatch compensated analogue buffer for driver-integrated poly-Si TFT LCDs. Electronics Letters, 2005, 41, 65.	0.5	10
74	Low-Phase Noise LC-tank Quadrature Voltage Controlled Oscillator. , 2005, , .		2
75	A low-ripple poly-Si TFT charge pump for driver-integrated LCD panel. IEEE Transactions on Consumer Electronics, 2005, 51, 606-610.	3.0	22
76	Digitally controlled phase locked loop with tracking analog-to-digital converter. , 2005, , .		2
77	Open-loop full-digital duty cycle correction circuit. Electronics Letters, 2005, 41, 635.	0.5	21
78	Characteristics of polyâ€Si TFTs required for Systemâ€onâ€Glass analog circuits. Journal of Information Display, 2004, 5, 1-6.	2.1	1
79	A 1.8-V 700-mb/s/pin 512-mb DDR-II SDRAM with on-die termination and off-chip driver calibration. IEEE Journal of Solid-State Circuits, 2004, 39, 941-951.	3.5	24
80	A common-gate switched 0.9-W class-E power amplifier with 41% PAE in 0.25-Î¼m CMOS. IEEE Journal of Solid-State Circuits, 2001, 36, 823-830.	3.5	148
81	A 2.5-V, 333-Mb/s/pin, 1-Gbit, double-data-rate synchronous DRAM. IEEE Journal of Solid-State Circuits, 1999, 34, 1589-1599.	3.5	17
82	A Â±1.5-V, 4-MHz CMOS continuous-time filter with a single-integrator based tuning. IEEE Journal of Solid-State Circuits, 1998, 33, 18-27.	3.5	48
83	A static power saving TTL-to-CMOS input buffer. IEEE Journal of Solid-State Circuits, 1995, 30, 616-620.	3.5	5
84	A low-power wide-bandwidth fully differential operational amplifier with current re-using feedforward frequency compensation. , 0, , .		12
85	Digital delay locked loop with open-loop digital duty cycle corrector for 1.2Gb/s/pin double data rate SDRAM. , 0, , .		12
86	Active-RC channel selection filter tunable from 6kHz to 18MHz for software-defined radio. , 0, , .		6
87	1.2V, 10MHz, low-pass Gm-C filter with Gm-cells based on triode-biased MOS and passive resistor in 0.13μm CMOS technology. , 0, , .		5