Katja Puschkarsky

List of Publications by Year
in descending order

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23	438	1163117 8	1281871 11
papers	citations	h-index	g-index

23	23	23	311
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Review on SiC MOSFETs High-Voltage Device Reliability Focusing on Threshold Voltage Instability. IEEE Transactions on Electron Devices, 2019, 66, 4604-4616.	3.0	101
2	Understanding BTI in SiC MOSFETs and Its Impact on Circuit Operation. IEEE Transactions on Device and Materials Reliability, 2018, 18, 144-153.	2.0	70
3	Investigation of threshold voltage stability of SiC MOSFETs. , 2018, , .		46
4	Understanding and modeling transient threshold voltage instabilities in SiC MOSFETs. , 2018, , .		36
5	Threshold voltage hysteresis in SiC MOSFETs and its impact on circuit operation. , 2017, , .		23
6	Impact of Mixed Negative Bias Temperature Instability and Hot Carrier Stress on MOSFET Characteristicsâ€"Part I: Experimental. IEEE Transactions on Electron Devices, 2019, 66, 232-240.	3.0	22
7	Physical Modeling of Charge Trapping in 4H-SiC DMOSFET Technologies. IEEE Transactions on Electron Devices, 2021, 68, 4016-4021.	3.0	22
8	NBTI Degradation and Recovery in Analog Circuits: Accurate and Efficient Circuit-Level Modeling. IEEE Transactions on Electron Devices, 2019, 66, 1662-1668.	3.0	18
9	Voltage-Dependent Activation Energy Maps for Analytic Lifetime Modeling of NBTI Without Time Extrapolation. IEEE Transactions on Electron Devices, 2018, 65, 4764-4771.	3.0	12
10	Circuit relevant HCS lifetime assessments at single transistors with emulated variable loads. , 2017, , .		11
11	Characterization and physical modeling of the temporal evolution of near-interfacial states resulting from NBTI/PBTI stress in nMOS/pMOS transistors. , 2018, , .		11
12	An Efficient Analog Compact NBTI Model for Stress and Recovery Based on Activation Energy Maps. IEEE Transactions on Electron Devices, 2019, 66, 4623-4630.	3.0	10
13	On the Physical Meaning of Single-Value Activation Energies for BTI in Si and SiC MOSFET Devices. IEEE Transactions on Electron Devices, 2021, 68, 236-243.	3.0	10
14	Implications of gate-sided hydrogen release for post-stress degradation build-up after BTI stress. , 2017, , .		9
15	Evaluation of Advanced MOSFET Threshold Voltage Drift Measurement Techniques. IEEE Transactions on Device and Materials Reliability, 2019, 19, 358-362.	2.0	9
16	The impact of mixed negative bias temperature instability and hot carrier stress on single oxide defects. , 2017, , .		8
17	The Impact of Interfacial Charge Trapping on the Reproducibility of Measurements of Silicon Carbide MOSFET Device Parameters. Crystals, 2020, 10, 1143.	2.2	6
18	NBTI: Experimental investigation, physical modelling, circuit aging simulations and verification. Microelectronics Reliability, 2018, 82, 1-10.	1.7	5

#	Article	IF	Citations
19	Fast acquisition of activation energy maps using temperature ramps for lifetime modeling of BTI. , 2018, , .		4
20	From Device Aging Physics to Automated Circuit Reliability Sign Off. , 2019, , .		3
21	Reliability and modeling: What to simulate and how?. , 2017, , .		2
22	Relevance of off-state NBTI degradation in depletion HVNMOS transistor for power application. , 2018, , .		0
23	Performance Analysis of 4H-SiC Pseudo-D CMOS Inverter Circuits Employing Physical Charge Trapping Models. Materials Science Forum, 0, 1062, 688-695.	0.3	0