Jaehun Jun

List of Publications by Year
in descending order

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79	1,255	430874	395702
papers	citations	18 h-index	33 g-index

79	79	79	1143
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A DCâ€“DC Boost Converter With Variation-Tolerant MPPT Technique and Efficient ZCS Circuit for Thermoelectric Energy Harvesting Applications. IEEE Transactions on Power Electronics, 2013, 28, 3827-3833.	7.9	134
2	A 0.15 V Input Energy Harvesting Charge Pump With Dynamic Body Biasing and Adaptive Dead-Time for Efficiency Improvement. IEEE Journal of Solid-State Circuits, 2015, 50, 414-425.	5.4	120
3	Self-Powered 30 ÂµW to 10 mW Piezoelectric Energy Harvesting System With 9.09 ms/V Maximum Power Point Tracking Time. IEEE Journal of Solid-State Circuits, 2015, 50, 2367-2379.	5.4	92
4	An Energy-Efficient Fast Maximum Power Point Tracking Circuit in an 800-Î¼W Photovoltaic Energy Harvester. IEEE Transactions on Power Electronics, 2013, 28, 2927-2935.	7.9	90
5	A 0.008 ${hbox {mm}}^{2}$ 500 $mu{m W}$ 469 kS/s Frequency-to-Digital Converter Based CMOS Temperature Sensor With Process Variation Compensation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2241-2248.	5.4	74
6	A 7 ps Jitter 0.053 mm<formula formulatype="inline"> <tex Notation="TeX">^{2}</tex></formula> Fast Lock All-Digital DLL With a Wide Range and High Resolution DCC. IEEE Journal of Solid-State Circuits, 2009, 44, 2437-2451.	5.4	58
7	A 1-mW Solar-Energy-Harvesting Circuit Using an Adaptive MPPT With a SAR and a Counter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 331-335.	3.0	36
8	3-Gb/s High-Speed True Random Number Generator Using Common-Mode Operating Comparator and Sampling Uncertainty of D Flip-Flop. IEEE Journal of Solid-State Circuits, 2017, 52, 605-610.	5.4	36
9	A 0.31â€“1 GHz Fast-Corrected Duty-Cycle Corrector With Successive Approximation Register for DDR DRAM Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1524-1528.	3.1	33
10	A Scalable Bandwidth Mismatch Calibration Technique for Time-Interleaved ADCs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1889-1897.	5.4	30
11	A 1.62 Gb/sâ€“2.7 Gb/s Referenceless Transceiver for DisplayPort v1.1a With Weighted Phase and Frequency Detection. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 268-278.	5.4	29
12	A 366kS/s 400uW 0.0013mm² frequency-to-digital converter based CMOS temperature sensor utilizing multiphase clock. , 2009, , .		28
13	A CMOS Magnetic Hall Sensor Using a Switched Biasing Amplifier. IEEE Sensors Journal, 2012, 12, 1195-1196.	4.7	28
14	A Single-Inductor Eight-Channel Output DCâ€“DC Converter With Time-Limited Power Distribution Control and Single Shared Hysteresis Comparator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 3354-3367.	5.4	26
15	A 100-nW 9.1-ENOB 20-kS/s SAR ADC for Portable Pulse Oximeter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 357-361.	3.0	24
16	Design and Implementation of Backtracking Wave-Pipeline Switch to Support Guaranteed Throughput in Network-on-Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 270-283.	3.1	23
17	366-kS/s 1.09-nJ 0.0013-${m mm}^{2}$ Frequency-to-Digital Converter Based CMOS Temperature Sensor Utilizing Multiphase Clock. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1950-1954.	3.1	22
18	A One-Cycle Lock Time Slew-Rate-Controlled Output Driver. , 2007, , .		21

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19	An Antiharmonic, Programmable, DLL-Based Frequency Multiplier for Dynamic Frequency Scaling. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1130-1134.	3.1	21
20	A 140-Mb/s to 1.82-Gb/s Continuous-Rate Embedded Clock Receiver for Flat-Panel Displays. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 773-777.	3.0	18
21	A 3.5 GHz Spread-Spectrum Clock Generator With a Memoryless Newton-Raphson Modulation Profile. IEEE Journal of Solid-State Circuits, 2012, 47, 1199-1208.	5.4	18
22	A Self-Calibrated DLL-Based Clock Generator for an Energy-Aware EISC Processor. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 575-579.	3.1	17
23	A 1-V 10-Gb/s/pin Single-Ended Transceiver With Controllable Active-Inductor-Based Driver and Adaptively Calibrated Cascaded-Equalizer for Post-LPDDR4 Interfaces. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 331-342.	5.4	15
24	A Single-Input Four-Output (SIFO) ACâ€“DC Rectifying System for Vibration Energy Harvesting. IEEE Transactions on Power Electronics, 2014, 29, 2629-2633.	7.9	13
25	A 6-bit 2.5-GS/s Time-Interleaved Analog-to-Digital Converter Using Resistor-Array Sharing Digital-to-Analog Converter. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2371-2383.	3.1	13
26	A 0.004-mm<formula formulatype="inline"><tex>^{2}</tex></formula> Portable Multiphase Clock Generator Tile for 1.2-GHz RISC Microprocessor. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 116-120.	3.0	12
27	A 1.62â€“5.4-Gb/s Receiver for DisplayPort Version 1.2a With Adaptive Equalization and Referenceless Frequency Acquisition Techniques. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2691-2702.	5.4	12
28	Fully Integrated Low-Power Energy Harvesting System With Simplified Ripple Correlation Control for System-on-a-Chip Applications. IEEE Transactions on Power Electronics, 2019, 34, 4353-4361.	7.9	12
29	Piecewise Linear Modulation Technique for Spread Spectrum Clock Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1234-1245.	3.1	11
30	A Novel Architecture for Block Interleaving Algorithm in MB-OFDM Using Mixed Radix System. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1020-1024.	3.1	10
31	An on-chip soft-start technique of current-mode DC-DC converter for biomedical applications. , 2010, , .		9
32	A low-voltage high-efficiency voltage doubler for thermoelectric energy harvesting. , 2013, , .		9
33	Design and Implementation of an On-Chip Permutation Network for Multiprocessor System-On-Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 173-177.	3.1	9
34	A TDC-based skew compensation technique for high-speed output driver. , 2012, , .		8
35	An On-Chip Network Fabric Supporting Coarse-Grained Processor Array. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 178-182.	3.1	8
36	A Periodically Refreshed Capacitive Floating Level Shifter for Conditional Switching Applications. IEEE Transactions on Power Electronics, 2021, 36, 1264-1268.	7.9	8

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37	A 250-Mb/s to 6-Gb/s Referenceless Clock and Data Recovery Circuit With Clock Frequency Multiplier. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 650-654.	3.0	7
38	A 5-GHz Subsampling PLL-Based Spread-Spectrum Clock Generator by Calibrating the Frequency Deviation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1132-1136.	3.0	7
39	A Four-Phase Hybrid Step-Up/Down Converter With RMS Inductor Current Reduction and Delay-Based Zero-Current Detection. IEEE Transactions on Power Electronics, 2022, 37, 3708-3712.	7.9	7
40	A 140 Mb/s to 1.96 Gb/s Referenceless Transceiver With 7.2 mus Frequency Acquisition Time. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1310-1315.	3.1	6
41	A 42 nJ/Conversion On-Demand State-of-Charge Indicator for Miniature IoT Li-Ion Batteries. IEEE Journal of Solid-State Circuits, 2019, 54, 524-537.	5.4	6
42	A 56-Gb/s PAM-4 Receiver Using Time-Based LSB Decoder and S/H Technique for Robustness to Comparator Voltage Variations. IEEE Journal of Solid-State Circuits, 2022, 57, 562-572.	5.4	6
43	A 7.5-Gb/s Referenceless Transceiver With Adaptive Equalization and Bandwidth-Shifting Technique for Ultrahigh-Definition Television in a 0.13- <inline-formula> <tex-math notation="TeX">$muhbox{m}$</tex-math></inline-formula> CMOS Process. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 865-869.	3.0	5
44	Physically Unclonable Function Using Ring Oscillator Collapse in 0.5 V Near-Threshold Voltage for Low-Power Internet of Things. , 2018, , .		5
45	24-Gb/s Input-Data-Independent Clock and Data Recovery Utilizing Bit-Efficient Braid Clock Signaling With Fixed Embedded Transition for 8K-UHD Intrapanel Interface. IEEE Solid-State Circuits Letters, 2019, 2, 21-24.	2.0	5
46	12-Gb/s Over Four Balanced Lines Utilizing NRZ Braid Clock Signaling With No Data Overhead and Spread Transition Scheme for 8K UHD Intra-Panel Interfaces. IEEE Journal of Solid-State Circuits, 2019, 54, 463-475.	5.4	5
47	Small-area high-accuracy ODT/OCD by calibration of global on-chip for 512M GDDR5 application. , 2009, , .		4
48	Current-mode DC-DC buck converter with reliable hysteretic-mode control and dual modulator for fast dynamic voltage scaling. , 2009, , .		4
49	A near-threshold all-digital PLL with a bootstrapped DCO using low-dropout regulator for mitigating PVT-variations. , 2017, , .		4
50	A Low-Power Post-LPDDR4 Interface Using AC Termination at RX and an Active Inductor at TX. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 789-793.	3.0	4
51	A 9-bit 500-MS/s 2-bit/cycle SAR ADC With Error-Tolerant Interpolation Technique. IEEE Journal of Solid-State Circuits, 2022, 57, 1492-1503.	5.4	4
52	A 15 Gb/s Non-Return-to-Zero Transmitter With 1-Tap Pre-Emphasis Feed-Forward Equalizer for Low-Power Ground Terminated Memory Interfaces. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2737-2741.	3.0	4
53	Experimental Demonstration of RoFSO Transmission Combining WLAN Standard and WDM-FSO over 100m Distance. , 2022, , .		4
54	A Compact and High Performance Switch for Circuit-Switched Network-On-Chip. , 2006, , .		3

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55	A DC-DC converter with a dual VCDL-based ADC and a self-calibrated DLL-based clock generator for an energy-aware EISC processor. , 2008, , .		3
56	A cost-effective design of spread spectrum clock generator. , 2010, , .		3
57	A 5-BIT 500-MS/S FLASH ADC USING TIME-DOMAIN COMPARISON. Journal of Circuits, Systems and Computers, 2012, 21, 1240023.	1.5	3
58	A 5.4Gb/s adaptive equalizer with unit pulse charging technique in 0.13µm CMOS. , 2012, , .		3
59	A <inline-formula> <tex-math notation="LaTeX">$4times 5$ </tex-math> </inline-formula>-Gb/s 1.12-<inline-formula> <tex-math notation="LaTeX">$mu ext{s}$ </tex-math> </inline-formula> Locking Time Reference-Less Receiver With Asynchronous Sampling-Based Frequency Acquisition and Clock Shared Subchannels. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2768-2777.	3.1	3
60	A 9 Gb/s/ch Transceiver With Reference-Less Data-Embedded Pseudo-Differential Clock Signaling for Graphics Memory Interfaces. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1982-1986.	3.0	3
61	An 88.9-dB SNR Fully-Dynamic Noise-Shaping SAR Capacitance-to-Digital Converter. IEEE Journal of Solid-State Circuits, 2022, 57, 2778-2790.	5.4	3
62	Analysis and evaluation of traffic-performance in a backtracked routing network-on-chip. , 2008, , .		2
63	10â€“315-MHz Cascaded Hybrid Phase-Locked Loop for Pixel Clock Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 2080-2093.	3.1	2
64	A 42nJ/conversion on-demand state-of-charge indicator for miniature IoT Li-ion batteries. , 2017, , .		2
65	A $DeltaSigma$ Modulator-Based Spread-Spectrum Clock Generator with Digital Compensation and Calibration for Phase-Locked Loop Bandwidth. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 192-196.	3.0	2
66	A 1-3.2 GHz 0.6 mW/GHz Duty-Cycle-Corrector Using Bangbang Duty-Cyle-Detector. , 2021, , .		2
67	Analysis of a Multiwire, Multilevel, and Symbol Correlation Combination Scheme. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 3416-3427.	5.4	2
68	A cost-effective design of non-linear modulation profile for spread spectrum clock. , 2012, , .		1
69	12Gb/s over four balanced lines utilizing NRZ braid clock signaling with 100% data payload and spread transition scheme for 8K UHD intra-panel interface. , 2018, , .		1
70	31% Reduction of power consumption using active inductor at TX and AC termination at RX for a low-power post-LPDDR4 interfaces. , 2018, , .		1
71	A Spread Spectrum Clock Generator With Nested Modulation Profile for a High-Resolution Display System. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1509-1513.	3.0	1
72	A 2.4â€“8 GHz Phase Rotator Delay-Locked Loop Using Cascading Structure for Direct Inputâ€“Output Phase Detection. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 794-798.	3.0	1

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73	Highâ€performance wideâ€•V DDH â€•range level converter for mixedâ€•signal systems. Electronics Letters, 2013, 49, 1125-1126.	1.0	0
74	Circuit design techniques for multimedia wireline communications. , 2015, , .		0
75	A digital low-dropout(DLDO) regulator with 14dB power supply rejection enhancement. , 2016, , .		0
76	A 10 Gbits/s/pin DFE-Less Graphics DRAM Interface With Adaptive-Bandwidth PLL for Avoiding Noise Interference and CIJ Reduction Technique. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 344-353.	3.1	0
77	A 1.3 V input fast-transient-response time digital low-dropout regulator with a VSSa generator for DVFS system. IEICE Electronics Express, 2017, 14, 20170461-20170461.	0.8	0
78	A Parasitics-Induced Failure Mechanism for Transistors in the Bit-Line Sense Amplifier Region of DDP DDR3 DRAM During a CDM Event. IEEE Transactions on Device and Materials Reliability, 2019, 19, 711-717.	2.0	0
79	A 0.37â€in. 5900PPI liquid crystal on silicon CMOS SoC using low voltage high dynamic voltage range novel pixel circuit for augmented reality microâ€displays. Journal of the Society for Information Display, 2021, 29, 785.	2.1	0