Ebrahim Farshidi

List of Publications by Year
in descending order

50 papers	**401** citations	1040056 **9** h-index	794594 **19** g-index
50 all docs	**50** docs citations	**50** times ranked	**359** citing authors

#	ARTICLE	IF	CITATIONS
1	A new approach for data augmentation in a deep neural network to implement a monitoring system for detecting prostate cancer in MRI images. Journal of Intelligent and Fuzzy Systems, 2022, , 1-16.	1.4	0
2	Design and Analysis of a Multirate 5-bit High-Order 52 fsrms Î" â˜ Time-to-Digital Converter Implemented on 40 nm Altera Stratix IV FPGA. IEEE Access, 2021, 9, 128117-128125.	4.2	1
3	An ultra-low power high-precision logarithmic-curvature compensated all-CMOS voltage reference in 65Ânm CMOS. Analog Integrated Circuits and Signal Processing, 2021, 107, 319-330.	1.4	1
4	Design and FPGA implementation of a multirate Î"â˜ time-to-digital converter with third-order noise-shaping. Microelectronics Journal, 2021, 108, 104982.	2.0	1
5	Low energy and area efficient quaternary multiplier with carbon nanotube field effect transistors. ETRI Journal, 2021, 43, 717-727.	2.0	1
6	Digital Calibration of Memory Errors in Passive Sigma-Delta Modulator. IETE Journal of Research, 2020, 66, 14-21.	2.6	2
7	Analysis, Design, and Implementation of a ZVT High Step-Up DCâ€"DC Converter With Continuous Input Current. IEEE Transactions on Industrial Electronics, 2020, 67, 10455-10463.	7.9	23
8	Novel CPG algorithm for tracking fast sudden changes based on tangent rule. International Journal of Electronics, 2020, 107, 930-950.	1.4	1
9	Digital calibration of pipelined ADC using Newtonâ€"Raphson algorithm. Analog Integrated Circuits and Signal Processing, 2020, 104, 61-70.	1.4	0
10	Novel design for a low-latency CORDIC algorithm for sine-cosine computation and its Implementation on FPGA. Microprocessors and Microsystems, 2020, 77, 103197.	2.8	8
11	Interleaved nonâ€isolated DCâ€"DC converter for ultraâ€high stepâ€up applications. IET Power Electronics, 2020, 13, 4261-4269.	2.1	8
12	Two-Stage Estimator for Frequency Rate and Initial Frequency in LFM Signal Using Linear Prediction Approach. Circuits, Systems, and Signal Processing, 2019, 38, 105-117.	2.0	6
13	A high precision logarithmic-curvature compensated all CMOS voltage reference. Analog Integrated Circuits and Signal Processing, 2019, 99, 383-392.	1.4	4
14	An FPGA-Based 16-Bit Continuous-Time 1-1 MASH Î"Î£ TDC Employing Multirating Technique. Electronics (Switzerland), 2019, 8, 1285.	3.1	4
15	A Split-Based Digital Background Calibration of Pipelined Analog-to-Digital Converters by Cubic Spline Interpolation Filtering. Circuits, Systems, and Signal Processing, 2019, 38, 4799-4816.	2.0	5
16	Robust reservoir rock fracture recognition based on a new sparse feature learning and data training method. Multidimensional Systems and Signal Processing, 2019, 30, 2113-2146.	2.6	18
17	A low power passive-active Î"Î£ modulator with high-resolution employing an integrator with open-loop unity-gain buffer. The Integration VLSI Journal, 2019, 64, 137-142.	2.1	2
18	A New Low Voltage Analog Circuit Model for Hodgkinâ€"Huxley Neuron Employing FGMOS Transistors. Journal of Circuits, Systems and Computers, 2018, 27, 1850141.	1.5	7

#	Article	IF	Citations
19	Stability enhancement of ITO-free non-inverted PTB7:PC71BM solar cell using two-step post-treated PEDOT:PSS. Journal of Materials Science: Materials in Electronics, 2018, 29, 12387-12398.	2.2	5
20	Role of hydrogen treatment on microstructural and opto-electrical properties of amorphous ITO thin films deposited by reactive gas-timing DC magnetron sputtering. Journal of Materials Science: Materials in Electronics, 2017, 28, 10525-10534.	2.2	3
21	All optical 2-bit analog to digital converter using photonic crystal based cavities. Optical and Quantum Electronics, 2017, 49, 1.	3.3	127
22	Effects of processing parameters on crystalline structure and optoelectronic behavior of DC sputtered ITO thin film. Journal of Materials Science: Materials in Electronics, 2017, 28, 787-797.	2.2	29
23	Detection of reservoir fractures in imaging logs using directional filtering. , 2017, , .		7
24	A fast locked and low phase noise all-digital phase locked loop based on model predictive control. Analog Integrated Circuits and Signal Processing, 2016, 88, 401-414.	1.4	2
25	Analysis of chaotic behavior in pipelined analog to digital converters. AEU - International Journal of Electronics and Communications, 2016, 70, 301-310.	2.9	9
26	A New Approach to Analysis and Design of Chaos-Based Random Number Generators Using Algorithmic Converter. Circuits, Systems, and Signal Processing, 2016, 35, 3830-3846.	2.0	19
27	A new digital background calibration for redundant radix-4 pipelined ADCs by modeling of adaptive filter for linear and nonlinear errors. Measurement: Journal of the International Measurement Confederation, 2016, 83, 123-134.	5.0	4
28	Analysis and Modeling of Imperfections in Multi-Bit Per Stage Pipelined ADCs. Journal of Circuits, Systems and Computers, 2016, 25, 1650079.	1.5	1
29	A new approach to analysis of residue probability density function in pipelined ADCs. The Integration VLSI Journal, 2016, 52, 51-61.	2.1	1
30	Design of a Novel Pipeline Time-to-Digital Converter Based on Dual-Slope Interpolation and Time Amplification. IETE Journal of Research, 2015, 61, 300-307.	2.6	4
31	A New Triple-Slope Pipelined Time to Digital Converter by Stretching of Time. Journal of Circuits, Systems and Computers, 2015, 24, 1550135.	1.5	2
32	A 5-bit time to digital converter using time to voltage conversion and integrating techniques for agricultural products analysis by Raman spectroscopy. Information Processing in Agriculture, 2014, 1, 124-130.	4.1	5
33	New systematic two‐graph‐based approach of active filters employing multiple output current controlled conveyors. IET Circuits, Devices and Systems, 2013, 7, 326-336.	1.4	3
34	A FG-MOS Based Fully Differential Current Controlled Conveyor and Its Applications. Circuits, Systems, and Signal Processing, 2013, 32, 993-1011.	2.0	18
35	A new fully differential second generation current controlled convey or using FG-MOS. , 2012, , .		0
36	A fast digital phase locked loop based on model predictive controller. , 2012, , .		1

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37	A new true RMS-to-DC converter using up-down translinear loop in CMOS technology. Analog Integrated Circuits and Signal Processing, 2012, 70, 385-390.	1.4	15
38	An Analog Template-Based Classifier Using MOS Translinear Loops. Active and Passive Electronic Components, 2011, 2011, 1-9.	0.3	4
39	A micropower current-mode pattern-matching classifier circuit using FG-MOS transistors. , 2009, , .		3
40	A low-voltage class-AB linear transconductance based on floating-gate MOS technology. , 2009, , .		2
41	A current-mode euclidean distance calculator based on electronically simulated translinear principle. , 2009, , .		0
42	A micropower current-mode sigma-delta modulator for biomedical applications. , 2009, , .		2
43	A systematic design procedure for floating-gate MOS based class-AB Log-domain filters. , 2009, , .		1
44	A 1.2V current-mode true RMSâ€"DC converter based on the floating gate MOS translinear principle. Microelectronics Journal, 2008, 39, 293-298.	2.0	25
45	A low-power current-mode defuzzifier for fuzzy logic controllers. , 2008, , .		6
46	Low-power current-mode linguistic-hedge circuits for fuzzy logic controllers. , 2008, , .		0
47	A systematic design procedure for log-domain filters based on nonlinear transconductance. , 2008, , .		3
48	A current-mode true RMS-DC converter based on electronically simulated translinear principle. , 2008, , .		3
49	Simple realization of CMOS current-Mode Wheatstone bridge. , 2008, , .		5
50	Low voltage second-order alpha function synapse. Analog Integrated Circuits and Signal Processing, 0, , .	1.4	0