Sridharan K

List of Publications by Year
in descending order

42 papers	1,230 citations	516710 16 h-index	552781 26 g-index
44 all docs	44 docs citations	44 times ranked	836 citing authors

#	Article	IF	Citations
1	A High-Performance VLSI Architecture for a Self-Feedback Convolutional Neural Network. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 456-460.	3.0	2
2	Low-Power and High-Performance Ternary SRAM Designs With Application to CNTFET Technology. IEEE Nanotechnology Magazine, 2021, 20, 562-566.	2.0	24
3	A Resource-Efficient Multiplierless Systolic Array Architecture for Convolutions in Deep Networks. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 370-374.	3.0	16
4	Protecting an Autonomous Delivery Agent Against a Vision-Guided Adversary: Algorithms and Experimental Results. IEEE Transactions on Industrial Informatics, 2020, 16, 5667-5679.	11.3	10
5	Interval Analysis Technique for Versatile and Parallel Multi-Agent Collision Detection and Avoidance. Journal of Intelligent and Robotic Systems: Theory and Applications, 2020, 98, 705-720.	3.4	7
6	CNTFET-Based Design of a Ternary Multiplier. Carbon Nanostructures, 2020, , 63-68.	0.1	0
7	Multiagent Gathering With Collision Avoidance and a Minimax Distance Criterionâ€"Efficient Algorithms and Hardware Realization. IEEE Transactions on Industrial Informatics, 2019, 15, 699-709.	11.3	3
8	Hardware-Efficient Velocity Estimation of Dynamic Obstacles Based on a Novel Radix-4 CORDIC and FPGA Implementation. , 2018, , .		3
9	Time Optimal Rendezvous for Multi-Agent Systems Amidst Obstacles - Theory and Experiments. , 2018, , .		0
10	Understanding the Incipient Discharge Activity with Epoxy/MoS<sub>2</sub> Nanocomposites. International Journal of the Society of Materials Engineering for Resources, 2018, 23, 195-202.	0.1	3
11	A Transistor-Level Probabilistic Approach for Reliability Analysis of Arithmetic Circuits With Applications to Emerging Technologies. IEEE Transactions on Reliability, 2017, 66, 440-457.	4.6	14
12	A Synthesis Methodology for Ternary Logic Circuits in Emerging Device Technologies. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2146-2159.	5.4	61
13	Carbon nanotube FETâ€based lowâ€delay and lowâ€power multiâ€digit adder designs. IET Circuits, Devices and Systems, 2017, 11, 352-364.	1.4	25
14	Real-Time SURF-Based Video Stabilization System for an FPGA-Driven Mobile Robot. IEEE Transactions on Industrial Electronics, 2016, , 1-1.	7.9	25
15	Rendezvous of heterogeneous robots amidst obstacles with limited communication. , 2016, , .		0
16	Low-Complexity Multiternary Digit Multiplier Design in CNTFET Technology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 753-757.	3.0	38
17	CORDIC-Based Azimuth Calculation and Obstacle Tracing via Optimal Sensor Placement on a Mobile Robot. IEEE/ASME Transactions on Mechatronics, 2016, 21, 2317-2329.	5.8	19
18	Hardware-Directed Feature Detection for Video Stitching in Intelligent Transportation. , 2015, , .		0

#	Article	IF	Citations
19	A Bit-Serial Pipelined Architecture for High-Performance DHT Computation in Quantum-Dot Cellular Automata. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2352-2356.	3.1	33
20	Reliability analysis of full adder in Schottky Barrier Carbon Nanotube FET technology. , 2014, , .		0
21	A pipelined architecture for motion tracking on a multicore environment. , 2014, , .		1
22	Efficient Multiternary Digit Adder Design in CNTFET Technology. IEEE Nanotechnology Magazine, 2013, 12, 283-287.	2.0	44
23	Efficient design of Baugh-Wooley multiplier in Quantum-Dot Cellular Automata. , 2013, , .		12
24	Efficient QCA design of single-bit and multi-bit subtractors. , 2013, , .		8
25	Low Complexity Design of Ripple Carry and Brentâ€"Kung Adders in QCA. IEEE Nanotechnology Magazine, 2012, 11, 105-119.	2.0	169
26	New Decomposition Theorems on Majority Logic for Low-Delay Adder Designs in Quantum Dot Cellular Automata. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 678-682.	3.0	39
27	Efficient VLSI Architectures for the Hadamard Transform Based on Offset-Binary Coding and ROM Decomposition. , 2011, , .		2
28	Efficient Design of a Hybrid Adder in Quantum-Dot Cellular Automata. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1535-1548.	3.1	69
29	Mobile Robot Navigation Through a Hardware-Efficient Implementation for Control-Law-Based Construction of Generalized Voronoi Diagram. IEEE/ASME Transactions on Mechatronics, 2011, 16, 1083-1095.	5.8	30
30	Robotic mapping with simple sensing and processing hardware — Algorithm and architecture. , 2010, , .		9
31	Hardware architecture for finding shortest paths. , 2009, , .		6
32	Efficient FPGA Realization of CORDIC With Application to Robotic Exploration. IEEE Transactions on Industrial Electronics, 2009, 56, 4915-4929.	7.9	34
33	50 Years of CORDIC: Algorithms, Architectures, and Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 1893-1907.	5.4	424
34	Efficient CORDIC Algorithms and Architectures for Low Area and High Throughput Implementation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 61-65.	3.0	51
35	A hardware-architecture for control-law based voronoi diagram computation and FPGA implementation. , 2008, , .		0
36	A novel CAM-based robotic indoor exploration algorithm and its area-efficient implementation. , 2008, , .		1

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37	The Design of a Hardware Accelerator for Real-Time Complete Visibility Graph Construction and Efficient FPGA Implementation. IEEE Transactions on Industrial Electronics, 2005, 52, 1185-1187.	7.9	20
38	A course on web languages and web-based applications. IEEE Transactions on Education, 2004, 47, 254-260.	2.4	11
39	Hardware-Efficient Schemes for Logarithmic Approximation and Binary Search With Application to Visibility Graph Construction. IEEE Transactions on Industrial Electronics, 2004, 51, 1346-1348.	7.9	2
40	A High-Speed VLSI Design and ASIC Implementation for Constructing Euclidean Distance-Based Discrete Voronoi Diagram. IEEE Transactions on Automation Science and Engineering, 2004, 20, 352-358.	2.3	9
41	An efficient fractals-based algorithm for clustering. , 0, , .		1
42	An efficient algorithm to construct reduced visibility graph and its FPGA implementation. , 0, , .		4