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List of Publications by Year in Descending Order

93 papers	1,714 citations	21 h-index	38 g-index
108 ext. papers	2,275 ext. citations	3.8 avg, IF	4.93 L-index

#	Paper	IF	Citations
93	IMCRYPTO: An In-Memory Computing Fabric for AES Encryption and Decryption. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2022**, 1-13	2.6	0
92	FeFET Multi-Bit Content-Addressable Memories for In-Memory Nearest Neighbor Search. *IEEE Transactions on Computers*, **2021**, 1-1	2.5	0
91	Computing-in-Memory Using Ferroelectrics: From Single-to Multi-Input Logic. *IEEE Design and Test*, **2021**, 1-1	1.4	0
90	Compact Single-Phase-Search Multistate Content-Addressable Memory Design Using One FeFET/Cell. *IEEE Transactions on Electron Devices*, **2021**, 68, 109-117	2.9	5
89	Exploiting FeFETs via Cross-Layer Design from In-memory Computing Circuits to Meta-Learning Applications **2021**,		1
88	In-Memory Nearest Neighbor Search with FeFET Multi-Bit Content-Addressable Memories **2021**,		4
87	Algorithmic Acceleration of B/FV-Like Somewhat Homomorphic Encryption for Compute-Enabled RAM. *Lecture Notes in Computer Science*, **2021**, 66-89	0.9	3
86	FeCAM: A Universal Compact Digital and Analog Content Addressable Memory Using Ferroelectric. *IEEE Transactions on Electron Devices*, **2020**, 67, 2785-2792	2.9	18
85	Modeling and Benchmarking Computing-in-Memory for Design Space Exploration **2020**,		6
84	A Novel TIGFET-based DFF Design for Improved Resilience to Power Side-Channel Attacks **2020**,		6
83	Seed-and-vote based in-memory accelerator for DNA read mapping **2020**,		5
82	A Device Non-Ideality Resilient Approach for Mapping Neural Networks to Crossbar Arrays **2020**,		2
81	SearcHD: A Memory-Centric Hyperdimensional Computing With Stochastic Training. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 2422-2433	2.5	20
80	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 2300-2313	2.6	2
79	The Impact of Ferroelectric FETs on Digital and Analog Circuits and Architectures. *IEEE Design and Test*, **2020**, 37, 79-99	1.4	6
78	A Computing-in-Memory Engine for Searching on Homomorphically Encrypted Data. *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, **2019**, 5, 123-131	2.4	7
77	An Energy Efficient Non-Volatile Flip-Flop based on CoMET Technology **2019**,		1

76	A Mixed Signal Architecture for Convolutional Neural Networks. *ACM Journal on Emerging Technologies in Computing Systems*, **2019**, 15, 1-26	1.7	5
75	Design and Analysis of an Ultra-Dense, Low-Leakage, and Fast FeFET-Based Random Access Memory Array. *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, **2019**, 5, 103-112	2.4	23
74	Nonvolatile Spintronic Memory Cells for Neural Networks. *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, **2019**, 5, 67-73	2.4	1
73	Design of Hardware-Friendly Memory Enhanced Neural Networks **2019**,		11
72	Ferroelectric FET Based In-Memory Computing for Few-Shot Learning **2019**,		12
71	Guest Editors□Introduction: Special Issue on Architecture Advances Enabled by Emerging Technologies. *IEEE Design and Test*, **2019**, 36, 5-6	1.4	
70	Energy-Efficient Convolutional Neural Network Based on Cellular Neural Network Using Beyond-CMOS Technologies. *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, **2019**, 5, 85-93	2.4	4
69	Ferroelectric ternary content-addressable memory for one-shot learning. *Nature Electronics*, **2019**, 2, 521-529	28.4	94
68	Ferroelectric FET Based TCAM Designs for Energy Efficient Computing **2019**,		1
67	An Ultra-Dense 2FeFET TCAM Design Based on a Multi-Domain FeFET Model. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2019**, 66, 1577-1581	3.5	33
66	Power and Area Efficient FPGA Building Blocks Based on Ferroelectric FETs. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 1780-1793	3.9	11
65	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 159-172	2.6	37
64	Computing with ferroelectric FETs: Devices, models, systems, and applications **2018**,		31
63	Scaling for edge inference of deep neural networks. *Nature Electronics*, **2018**, 1, 216-222	28.4	149
62	Design and optimization of FeFET-based crossbars for binary convolution neural networks **2018**,		21
61	A ferroelectric field effect transistor based synaptic weight cell. *Journal Physics D: Applied Physics*, **2018**, 51, 434001	3	68
60	Biomedical Image Segmentation Using Fully Convolutional Networks on TrueNorth **2018**,		3
59	Nonvolatile Lookup Table Design Based on Ferroelectric Field-Effect Transistors **2018**,		8

58	Computing in memory with FeFETs **2018**,		29
57	Cross-layer efforts for energy-efficient computing: towards peta operations per second per watt. *Frontiers of Information Technology and Electronic Engineering*, **2018**, 19, 1209-1223	2.2	2
56	Can beyond-CMOS devices illuminate dark silicon?. *Communications of the ACM*, **2018**, 61, 60-69	2.5	3
55	Cellular neural network friendly convolutional neural networks CNNs with CNNs **2017**,		8
54	Advanced spintronic memory and logic for non-volatile processors **2017**,		10
53	Design and benchmarking of ferroelectric FET based TCAM **2017**,		34
52	Exploiting Non-Volatility for Information Processing **2017**,		2
51	Design of Stochastic Computing Circuits Using Nanomagnetic Logic. *IEEE Nanotechnology Magazine*, **2016**, 15, 179-187	2.6	5
50	Design of latches and flip-flops using emerging tunneling devices **2016**,		5
49	Can beyond-CMOS devices illuminate dark silicon? **2016**,		5
48	Exploiting ferroelectric FETs for low-power non-volatile logic-in-memory circuits **2016**,		36
47	Fabrication of pseudo-spin-valve giant magnetoresistance arrays for nanomagnet logic by liftoff and the snow-jet process. *Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics*, **2015**, 33, 022801	1.3	1
46	Error analysis for ultra dense nanomagnet logic circuits. *Journal of Applied Physics*, **2015**, 117, 17A906	2.5	8
45	TFET-based Operational Transconductance Amplifier Design for CNN Systems **2015**,		5
44	Better computing with magnets - The simple bar magnet, shrunk down to the nanoscale, could be a powerful logic device. *IEEE Spectrum*, **2015**, 52, 44-60	1.7	15
43	Analog Circuit Design Using Tunnel-FETs. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2015**, 62, 39-48	3.9	73
42	Analytically modeling power and performance of a CNN system **2015**,		2
41	A CNN-inspired mixed signal processor based on tunnel transistors **2015**,		1

40	Magnetic devices: clocking with no field. *Nature Nanotechnology*, **2014**, 9, 14-5	28.7	9
39	Design of 3D nanomagnetic logic circuits: A full-adder case study **2014**,		1
38	Contiguous clock lines for pipelined nanomagnet logic. *Journal of Computational Electronics*, **2014**, 13, 763-768	1.8	1
37	Impact of steep-slope transistors on non-von Neumann architectures: CNN case study **2014**,		2
36	Threshold Gate-Based Circuits From Nanomagnetic Logic. *IEEE Nanotechnology Magazine*, **2014**, 13, 990-996	2.6	11
35	Nontraditional Computation Using Beyond-CMOS Tunneling Devices. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2014**, 4, 438-449	5.2	13
34	Cellular neural networks for image analysis using steep slope devices **2014**,		2
33	Leveraging Emerging Technology for Hardware Security - Case Study on Silicon Nanowire FETs and Graphene SymFETs **2014**,		32
32	Nanomagnet Logic Gate With Programmable-Electrical Input. *IEEE Transactions on Magnetics*, **2014**, 50, 1-4	2	3
31	Impact of steep-slope transistors on non-von Neumann architectures: CNN case study **2014**,		2
30	Experimental Realization of a Nanomagnet Full Adder Using Slanted-Edge Magnets. *IEEE Transactions on Magnetics*, **2013**, 49, 4452-4455	2	37
29	Switching Behavior of Sharply Pointed Nanomagnets for Logic Applications. *IEEE Transactions on Magnetics*, **2013**, 49, 3549-3552	2	12
28	A Nanomagnet Logic Field-Coupled Electrical Input. *IEEE Nanotechnology Magazine*, **2013**, 12, 734-742	2.6	5
27	GPU acceleration of Data Assembly in Finite Element Methods and its energy implications **2013**,		4
26	Systematic design of Nanomagnet Logic circuits **2013**,		2
25	TFET-based cellular neural network architectures **2013**,		18
24	Systolic Pattern Matching Hardware With Out-of-Plane Nanomagnet Logic Devices. *IEEE Nanotechnology Magazine*, **2013**, 12, 399-407	2.6	30
23	Power reduction in nanomagnet logic using high-permeability dielectrics. *Journal of Applied Physics*, **2013**, 113, 17B906	2.5	6

22	Exploring the Design of the Magnetic□lectrical Interface for Nanomagnet Logic. *IEEE Nanotechnology Magazine*, **2013**, 12, 203-214	2.6	8
21	. *IEEE Transactions on Magnetics*, **2012**, 48, 3292-3295	2	15
20	Direct Measurement of Magnetic Coupling Between Nanomagnets for Nanomagnetic Logic Applications. *IEEE Transactions on Magnetics*, **2012**, 48, 4402-4405	2	11
19	Power reduction in nanomagnetic logic clocking through high permeability dielectrics **2012**,		1
18	Nanomagnet logic: progress toward system-level integration. *Journal of Physics Condensed Matter*, **2011**, 23, 493202	1.8	128
17	Magnetic□lectrical Interface for Nanomagnet Logic. *IEEE Nanotechnology Magazine*, **2011**, 10, 757-763	2.6	26
16	Experimental Demonstration of Fanout for Nanomagnetic Logic. *IEEE Nanotechnology Magazine*, **2010**, 9, 668-670	2.6	42
15	On-Chip Clocking for Nanomagnet Logic Devices. *IEEE Nanotechnology Magazine*, **2010**, 9, 348-351	2.6	113
14	Design and comparison of NML systolic architectures **2010**,		18
13	System-level energy and performance projections for nanomagnet-based logic **2009**,		12
12	Controlling Magnetic Circuits: How Clock Structure Implementation will Impact Logical Correctness and Power **2009**,		9
11	Non-volatile and reprogrammable MQCA-based majority gates **2009**,		14
10	PLAs in Quantum-Dot Cellular Automata. *IEEE Nanotechnology Magazine*, **2008**, 7, 376-386	2.6	19
9	Fabrication Variations and Defect Tolerance for Nanomagnet-Based QCA **2008**,		13
8	Bridging the gap between nanomagnetic devices and circuits **2008**,		8
7	Defect tolerance in QCA-based PLAs **2008**,		7
6	Design Tradeoffs for Improved Performance in MQCA-Based Systems **2008**,		4
5	Fault Models and Yield Analysis for QCA-Based PLAs **2007**,		11

4	Fabricatable Interconnect and Molecular QCA Circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 1978-1991	2.5	40
3	Clocking scheme for nanomagnet QCA **2007**,		14
2	Quantum-Dot Cellular Automata (QCA) circuit partitioning **2004**,		21
1	Problems in designing with QCAs: Layout = Timing. *International Journal of Circuit Theory and Applications*, **2001**, 29, 49-62	2	138